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A novel method to reduce differential crosstalk in a high-speed channel

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Abstract

This paper presents a new technique to minimize differential crosstalk in a high-speed channel by adjusting its four individual single-ended terms. This adjustment can be achieved by simply re-arranging the relative location of signal conductors such that the four single-ended crosstalk terms either cancel each other within an electrical component or give opposite polarities in differential crosstalk among several electrical components in a channel. In the latter case, the aggregate crosstalk of an entire channel is reduced from the largest crosstalk of individual components as a result.

Optimized via patterns, shown through both simulation and measurement, are used as examples to give minimum crosstalk in the vias, in the via-connector-via transition and/or in the entire channel. Upon understanding the polarity of each component's crosstalk, one can select the proper via configuration to improve a channel's insertion-loss-to-crosstalk-ratio (ICR) by more than 10dB.

The techniques presented in this paper can be applied to design packages, connectors, vias and traces for minimal crosstalk by themselves or to properly layout vias and traces for minimal crosstalk in an entire channel.

Authors Biography

Kunia Aihara is a Signal Integrity Engineer in the High-Speed Interconnect section at Hirose Electric USA, Inc. Prior to joining Hirose, he was with the U.S. Air Force Research Laboratory as an Electronics Engineer specializing in RF subsystems, modules and packaging. He received his B.S., M.S., and Ph.D. degrees in Electrical and Computer Engineering from University of California, Davis, in 2003, 2007 and 2008, respectively. He has authored and co-authored more than 25 technical conference papers, journals, book chapter and a book (titled "LCP for Microwave Packages and Modules," from Cambridge University Press).

Jeremy Buan is a Signal Integrity Engineer in the High-Speed Interconnect section at Hirose Electric USA, Inc. As an SI Engineer, he supports the development of high-speed connectors by both simulation and measurement. He gives SI/design assistance to customers by providing connector models, evaluation boards, channel simulation data and via breakout optimization. Jeremy received his BSEE and MSEE from San Jose State University.

Adam Nagao is a Signal Integrity Engineer in the High-Speed Interconnect section at Hirose Electric USA, Inc. His primary focus is on methods to characterize various interconnect products. He received his BSEE from Texas A&M University.

Toshi Takada is a Signal Integrity Manager in the High-Speed Interconnect section at Hirose Electric USA, Inc. He joined Hirose in 1996 as a connector development engineer for computer and telecom market. He received his B.S. Physics from Gakushuin University, Tokyo, Japan.

Ching-Chao Huang, President of AtaiTec Corp., has more than 25 years of high-speed connector, package and system design, and SI software development experience. He held such positions as advisory engineer at IBM, R&D manager at TMA, SI manager at Rambus, and Sr. VP at Optimal. Dr. Huang is an IEEE senior member and he has many patents and publications. Dr. Huang received his BSEE from National Taiwan University, and MSEE and PhD from Ohio State University.

1. Introduction

As exemplified by the insertion-loss-to-crosstalk-ratio (ICR) specification that appears in various IEEE802.3 standards, differential crosstalk is known to be one of the biggest limiters in channel performance. Previously, crosstalk has been controlled through isolation and/or separation [1], balance of inductive and capacitive coupling [2] and, more recently, polarity swapping [3]. This paper presents a new technique to minimize differential crosstalk by adjusting its four single-ended terms. This adjustment can be achieved by simply re-arranging the relative location of signal conductors such that the four single-ended crosstalk terms either cancel each other within an electrical component or give opposite polarities in differential crosstalk among several electrical components in a channel. In the latter case, aggregate crosstalk of an entire channel is reduced as a result.

In Section 2, we will examine the four single-ended terms that make up the differential crosstalk and explain why changing the relative location between two sets of vias and controlling their single-ended crosstalks can vary their differential NEXT and FEXT from one polarity to another [4]. In particular, if two sets of vias are arranged to be edge-coupled, their differential NEXT (or FEXT) is found to have negative (or positive) polarity. If two sets of vias are arranged to be broadside-coupled, their differential NEXT (or FEXT) is found to have positive (or negative) polarity. Thus, there exists a structure, akin to staggered broadside-coupled vias with optimal offset, which gives nearly zero differential NEXT or FEXT. It is apparent that pairing vias of opposite polarity with other components will improve a channel's total crosstalk.

To verify the above predictions, three test structures were fabricated and their simulation vs. measurement correlation is shown in Section 3. The first test structure corresponds to staggered broadside-coupled vias with various offsets. For direct comparison with HFSS [5] simulation, all test structures were de-embedded by In-Situ De-embedding [6]. The polarity of NEXT and FEXT can be clearly seen to depend on the offset. The minimum magnitudes of NEXT and FEXT are also shown to occur at certain offsets. The second test structure is for edge-coupled vias and broadside-coupled vias in cascade. Both simulation and measurement show that their differential crosstalks do cancel each other.

In the third test structure, we try to minimize differential FEXT in a via-connector-via transition. Hirose's IT9 connector is used as an example. In this case, we want to maximize, rather than minimize, via crosstalk to cancel connector's crosstalk. To increase the via crosstalk, some ground vias were removed. This gives such additional advantage as more routing space and improved power distribution around a connector. The insertion-loss-to-crosstalk-ratio (ICR) of via-connector-via transition has been shown to improve by more than 10 dB with proper via design.

While the first structure shows that we can minimize differential crosstalk within a component itself, the second and third structures verify that we can minimize differential crosstalk across multiple components. The techniques presented in this paper

can be applied to design packages, connectors, vias and traces for minimal crosstalk by themselves or to properly layout vias and traces for minimal crosstalk in an entire channel.

2. Theory

Time domain analysis can provide valuable information that one cannot immediately interpret from frequency domain response. Of particular interest is the polarity of crosstalk. The polarity information will be utilized to optimize crosstalk within a component or across multiple components. To illustrate the polarity of crosstalk, the edge-coupled and broadside-coupled vias are used as examples in the following.

2.1 Edge-coupled vias

Figure 1 illustrates two differential via pairs in edge-coupled configuration where the two pairs are in line with each other. Let Ports 1, 2, 5, 6 denote the first pair and Ports 3, 4, 7, 8 denote the second pair. Using HFSS for simulation and ADK [7] for post-processing, Figure 2 shows that, for a step input at Port 1 or 2, the single-ended NEXTs (S_{31} , S_{41} , S_{32} , S_{42}) are of the same (i.e., positive) polarity and the single-ended FEXTs (S_{71} , S_{72} , S_{81} , S_{82}) are of opposite (i.e., negative) polarity. (All time-domain step responses for the rest of this paper are created by ADK with 1 volt input and 50ps rise time (20% to 80%).) Due to the close proximity of vias with Ports 2->6 to 3->7, the single-ended terms of S_{32} and S_{72} dominate in the following differential NEXT (SDD21) and FEXT (SDD41) equations:

$$\begin{aligned} SDD21 &= \frac{1}{2}(S_{31} - S_{41} - S_{32} + S_{42}) \\ SDD41 &= \frac{1}{2}(S_{71} - S_{81} - S_{72} + S_{82}) \end{aligned} \quad (1)$$

As a result, SDD21 has negative polarity and SDD41 has positive polarity.

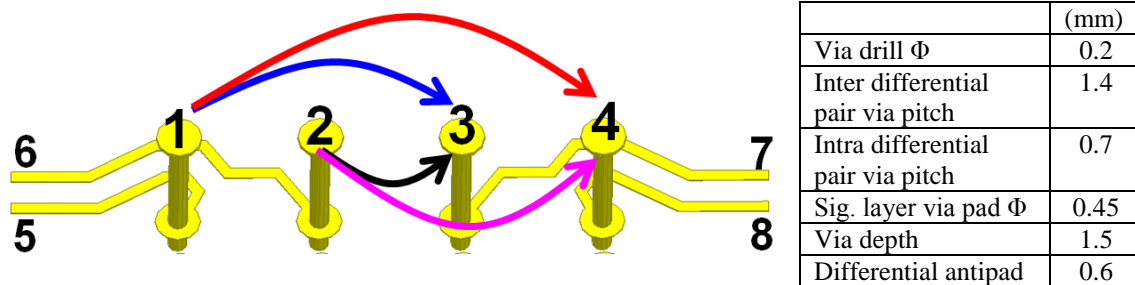


Figure 1. Edge-coupled differential vias.

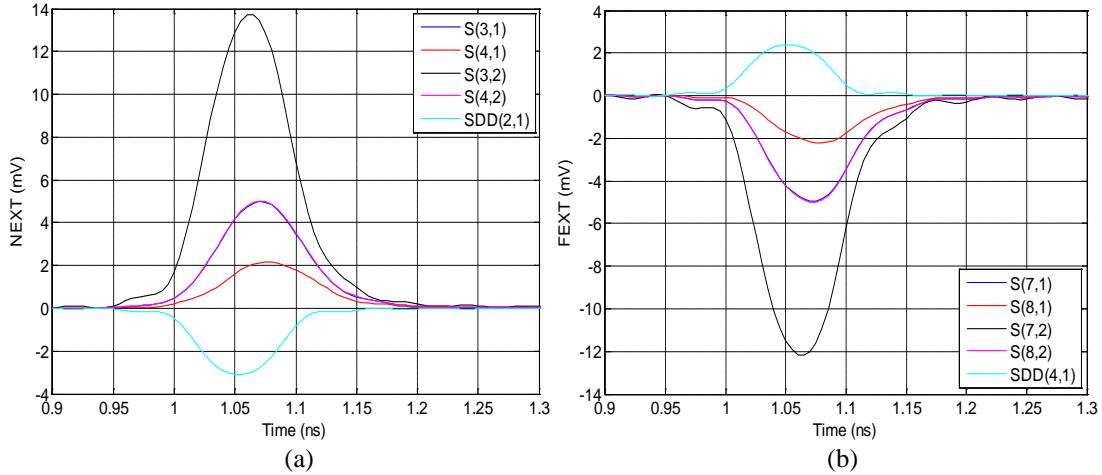
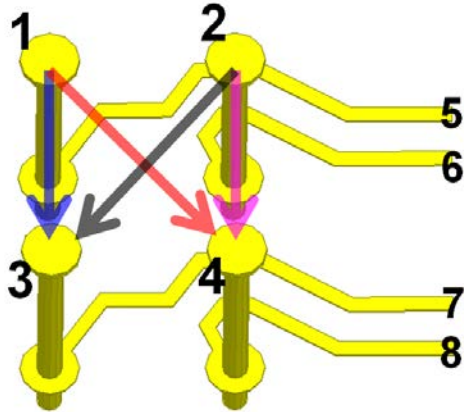


Figure 2. Single-ended and differential (a) NEXT and (b) FEXT of edge-coupled differential vias.

2.2 Broadside-coupled vias

Figure 3 illustrates two differential via pairs in broadside-coupled configuration where the two pairs are facing each other. Again, let Ports 1, 2, 5, 6 denote the first pair and Ports 3, 4, 7, 8 denote the second pair. As shown in Figure 4, for a step input at Port 1 or 2, we will have single-ended NEXT (S31, S41, S32, S42) of the same (i.e., positive) polarity and single-ended FEXT (S71, S72, S81, S82) of opposite (i.e., negative) polarity. Due to the close proximity of vias with Ports 1->5 to 3->7 and 2->6 to 4->8, the single-ended terms of S31, S42, S71 and S82 dominate in the differential NEXT (SDD21) and FEXT (SDD41) equations (see Eq. (1)). As a result, SDD21 has positive polarity and SDD41 has negative polarity.



	(mm)
Via drill Φ	0.2
Inter differential pair via pitch	1.75
Intra differential pair via pitch	0.7
Sig. layer via pad Φ	0.45
Via depth	1.5
Differential antipad	0.6

Figure 3. Broadside-coupled differential vias

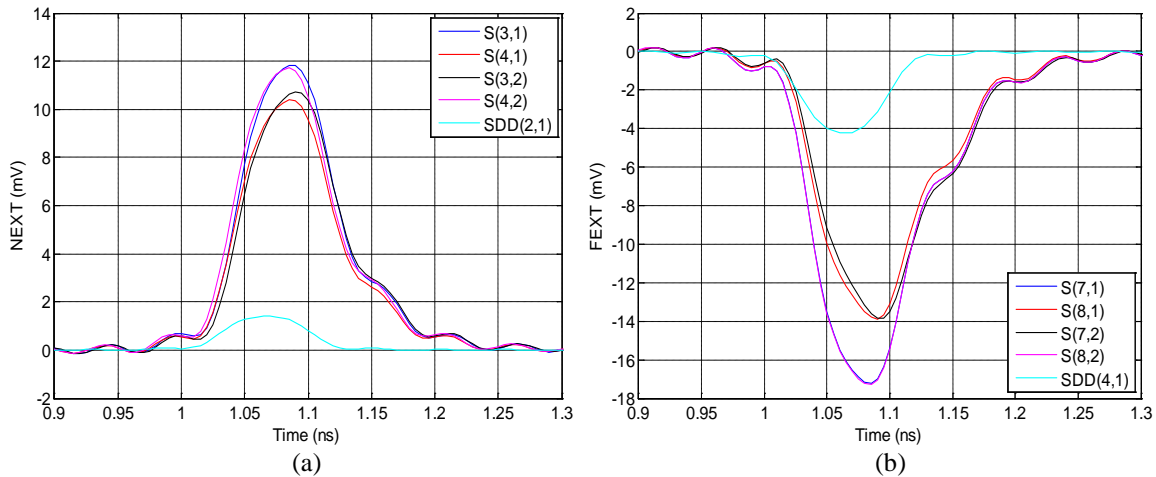


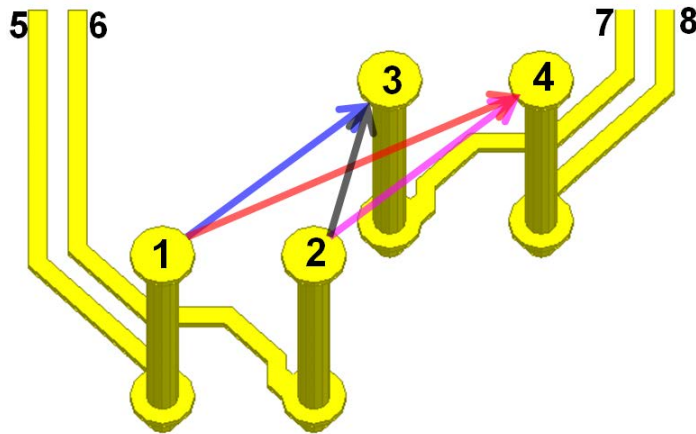
Figure 4. Single-ended and differential (a) NEXT and (b) FEXT of broadside-coupled differential vias.

2.3 Broadside-coupled vias with offset

To minimize SDD21 in Eq. (1), one can make $S_{31}+S_{42}$ approximately equal to $S_{41}+S_{32}$. (Similarly, to minimize SDD41, one can make $S_{71}+S_{82}$ approximately equal to $S_{81}+S_{72}$.) When two coupled differential pairs are far apart from each other, not only each single-ended crosstalk term becomes smaller but also $S_{31}+S_{42} \approx S_{41}+S_{32}$ and $S_{71}+S_{82} \approx S_{81}+S_{72}$, resulting in small SDD21 and SDD41. Larger spacing is not practical in many, if not most, cases, however.

The main contribution of this paper is to minimize SDD21 (and SDD41) either at the component level or for the entire channel. In so doing, we examine structures that give $S_{31}+S_{42} \approx S_{41}+S_{32}$ and $S_{71}+S_{82} \approx S_{81}+S_{72}$. These structures may require that certain single-ended crosstalk terms be increased in order to reduce the differential crosstalk.

One example to minimize the differential via crosstalk itself is to morph the edge-coupled vias with broadside-coupled vias, now that they give differential crosstalk of opposite polarity. This leads to the structure in Figure 5 which resembles broadside-coupled vias with offset. In this configuration, via 1->5 is brought closer to via 4->8, resulting in larger S41 and S81, but smaller SDD21 and SDD41, than the broadside-coupled configuration. At an optimal offset, shown in Figure 6, SDD21 and SDD41 can be made nearly 0.



	(mm)
Via drill Φ	0.2
Inter differential pair via pitch	Sec.3.1
Intra differential pair via pitch	0.7
Sig. layer via pad Φ	0.45
Via depth	1.5
Differential antipad	0.6

Figure 5. Broadside-coupled differential vias with offset

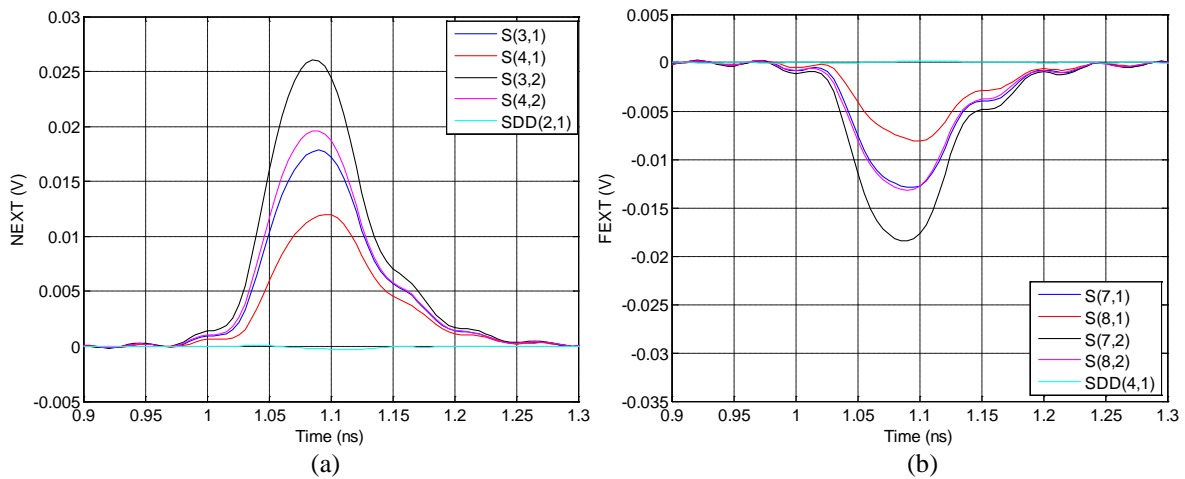


Figure 6. Single-ended and differential (a) NEXT and (b) FEXT of broadside-coupled differential vias with offset.

3. Test structures

To verify the above observations, three test structures were fabricated and measured. Figure 7 shows the PCB cross section of all test fixtures used in this paper. The material is FR408 and there are 8 metal layers (with 4 signal and 4 ground layers). 8mil and 12mil drills were used for the signal and ground vias, respectively. Layer S2, which is located 22mil below the top layer, is used to route all stripline signals. Thus, all signal vias are ~22mils plus via stub length at the connector via field. The target backdrill stub length is 20mil. For better de-embedding, vias were manually backdrilled further when needed.

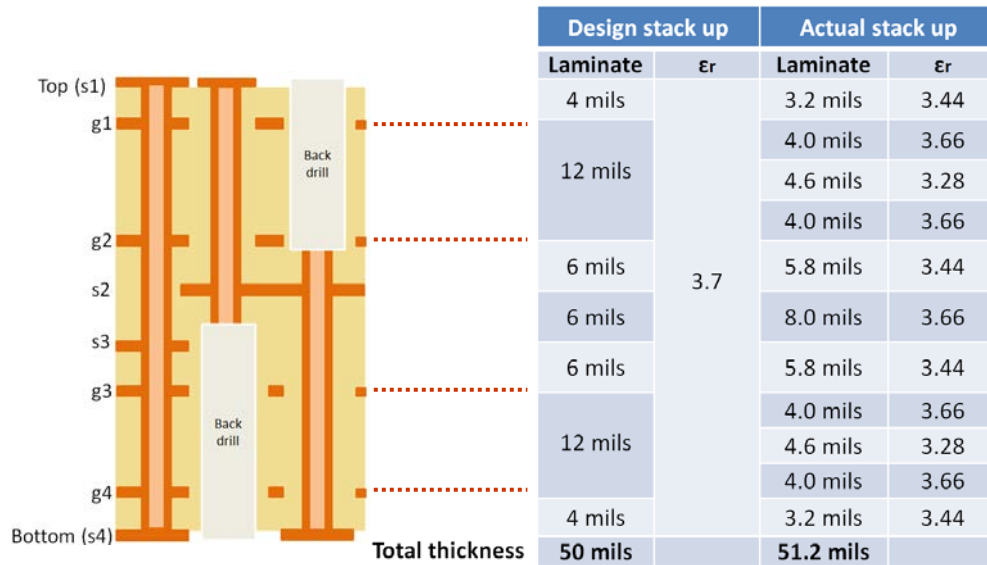


Figure 7. PCB cross section

3.1 Broadside-coupled vias with offset

The first test structure, shown in Figure 8, corresponds to staggered broadside-coupled vias with various offsets. Keeping the vertical separation at 1.05 mm, we measured several sets of vias with $\alpha=0^\circ$, 33.6° , 38.9° , 42.7° and 62.1° . In addition, edge-coupled vias, with the same horizontal distance as $\alpha=62.1^\circ$, are measured and denoted as $\alpha=90^\circ$.

For direct comparison with HFSS simulation, all test structures in this paper were de-embedded by AtaiTec's In-Situ De-embedding (ISD) software [6]. Unlike TRL calibration that uses multiple test coupons directly for de-embedding, ISD uses only one 2x thru test coupon as a reference and goes through optimization to de-embed the test fixture's actual impedance. As a result, ISD is able to give causal device-under-test (DUT) results that are easier to correlate [8].

Figure 9 shows good agreement between simulated and measured differential NEXT in frequency domain. Their time-domain step responses, with 1 volt input and 50ps rise time (20% to 80%), are shown in Figure 10. It is seen that the differential NEXT goes

from positive polarity at $\alpha=0^\circ$ to negative polarity at $\alpha=90^\circ$ and the minimum magnitude occurs at $\alpha=38.9^\circ$.

Similarly, Figure 11 shows good agreement between simulated and measured differential FEXT in frequency domain. Their time-domain step responses, with 1 volt input and 50ps rise time (20% to 80%), are shown in Figure 12. It is seen that the differential FEXT goes from negative polarity at $\alpha=0^\circ$ to positive polarity at $\alpha=90^\circ$ and the minimum magnitude occurs at $\alpha=42.7^\circ$.

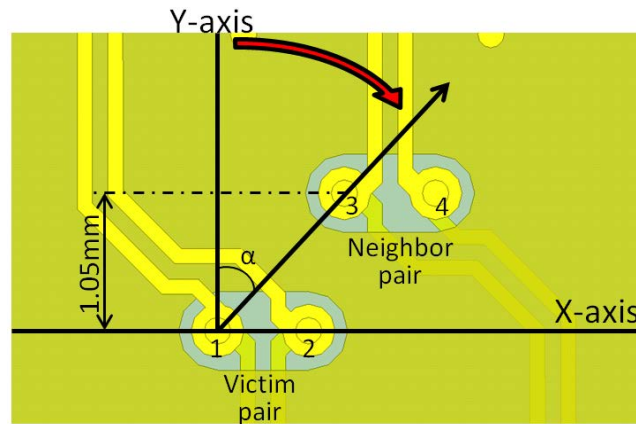


Figure 8. Broadside-coupled differential vias with offset.

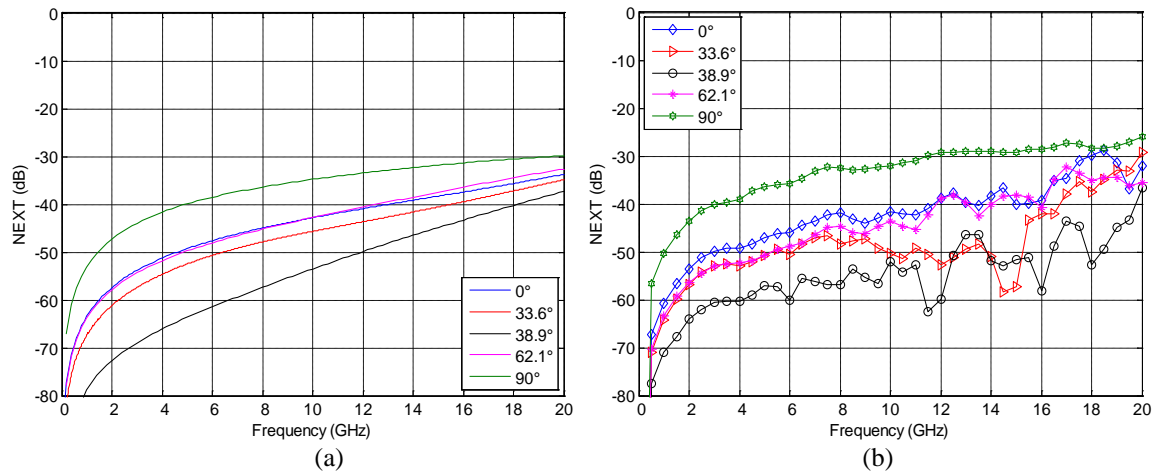


Figure 9. Frequency-domain differential NEXT of broadside-coupled vias with offset. (a) Simulation vs. (b) measurement.

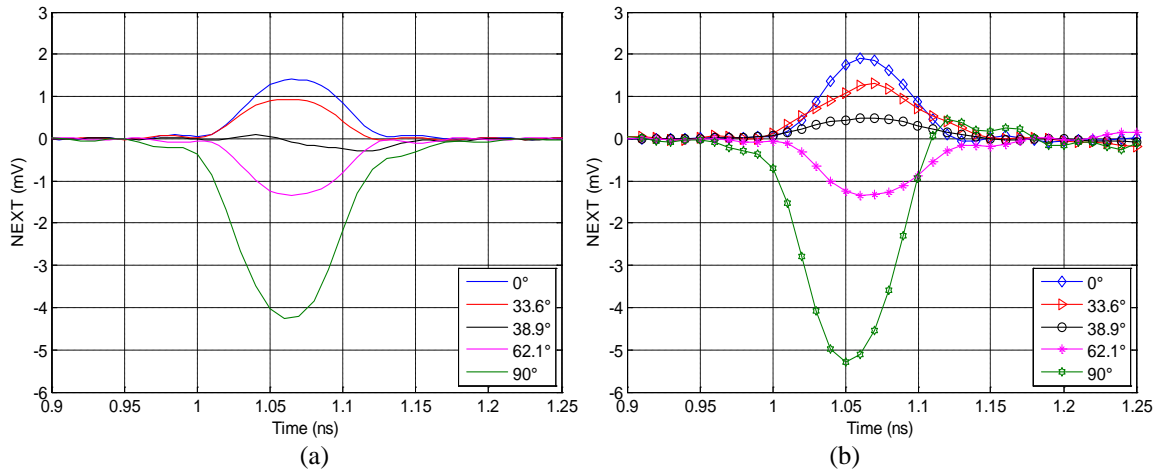


Figure 10. Time-domain differential NEXT of broadside-coupled vias with offset. (a) Simulation vs. (b) measurement.

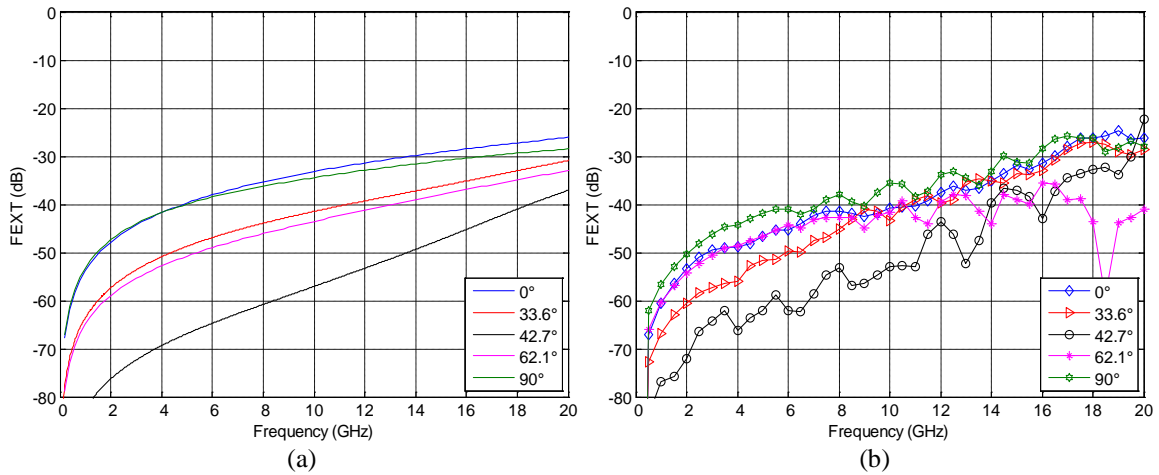


Figure 11. Frequency-domain differential FEXT of broadside-coupled vias with offset. (a) Simulation vs. (b) measurement.

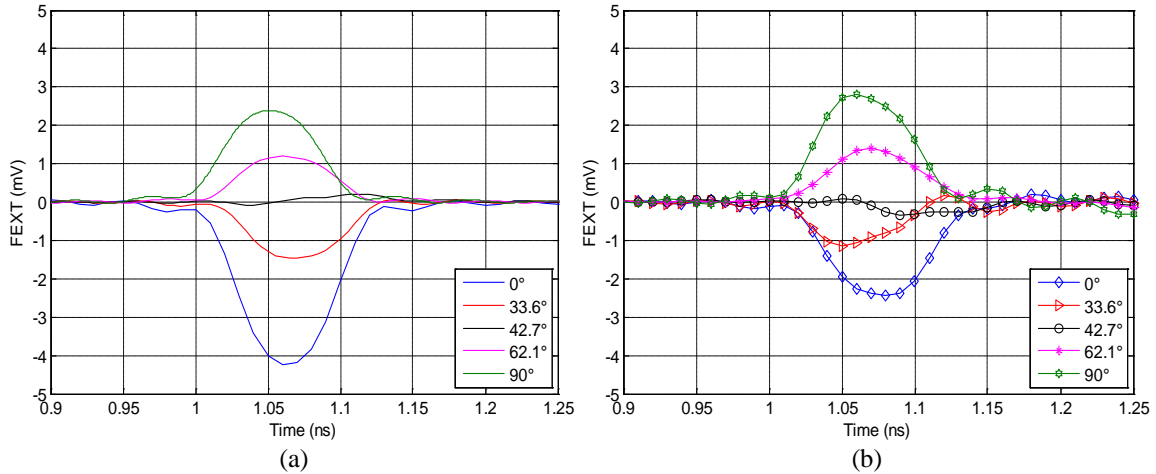


Figure 12. Time-domain differential FEXT of broadside-coupled vias with offset. Simulation (a) vs. measurement (b).

3.2 Edge-coupled vias and broadside-coupled vias in cascade

The second test structure, shown in Figure 13, puts edge-coupled vias and broadside-coupled vias in cascade, in order to demonstrate the cancellation effect of differential crosstalk across multiple components. Some ground vias are placed in the vicinity to avoid resonances and to isolate the fields of edge-coupled vias from the broadside-coupled vias.

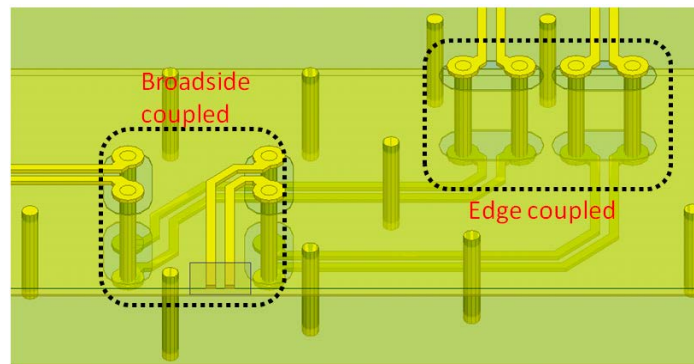


Figure 13. Edge-coupled and broadside-coupled vias in cascade.

Figure 14 shows an agreement between simulated and measured differential FEXT in frequency domain in that cancellation indeed occurs. Their time-domain step responses, with 1 volt input and 50ps rise time (20% to 80%), are shown in Figure 15. The edge-coupled-vias-only and broadside-coupled-vias-only results, same as Figure 11 and Figure 12, are plotted again in the same graphs to show the crosstalk cancellation at work.

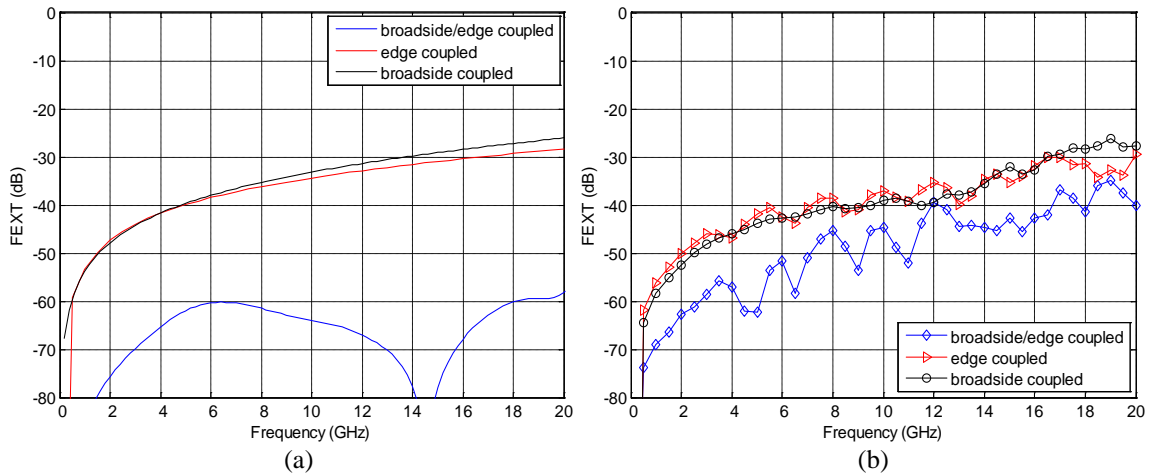


Figure 14. Frequency-domain differential FEXT of edge-coupled vias and broadside-coupled vias in cascade. (a) Simulation vs. (b) measurement.

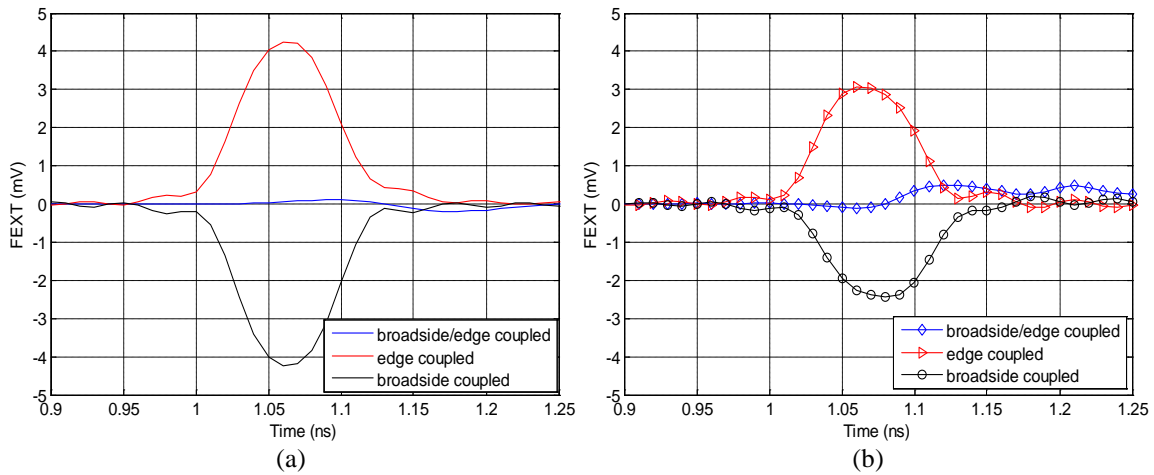


Figure 15. Time-domain differential FEXT of edge-coupled vias and broadside-coupled vias in cascade. Simulation (a) vs. measurement (b).

3.3 Via-connector-via transition

The third test structure, shown in Figure 16, uses Hirose's IT9-38H mezzanine connector to demonstrate how one can minimize crosstalk in an entire channel through proper via design. Being a 2-row surface-mount connector, IT9-38H has the largest crosstalk from the same-row neighboring aggressor. Figure 17 shows its simulated differential FEXT in GSSG (G=ground, S=signal) pin assignment. The time-domain step response was created with 1 volt input and 50ps rise time (20% to 80%). It is interesting to note that the same-

row aggressor and victim pairs are of edge-coupling type and they again give rise to FEXT of positive polarity. Similarly, the opposite-row aggressor and victim pairs are broadside-coupled and they give rise to FEXT of negative polarity. The large separation between two opposite rows makes this broadside coupling relatively small, however.

To cancel IT9-38H's FEXT of positive polarity, broadside-coupled vias with offset, shown in Figure 18, are built into the board. Such variables as offset, via depth, inter-pair pitch, intra-pair pitch, drill diameter and dielectric constant can all affect the crosstalk. In this design, the via depth, inter-pair pitch, intra-pair pitch and drill diameter are set to 0.6mm, 1.5mm, 1.27mm and 10mil, respectively. The dielectric constant is assumed to be 3.7 and the optimized offset is set to 0.75mm.

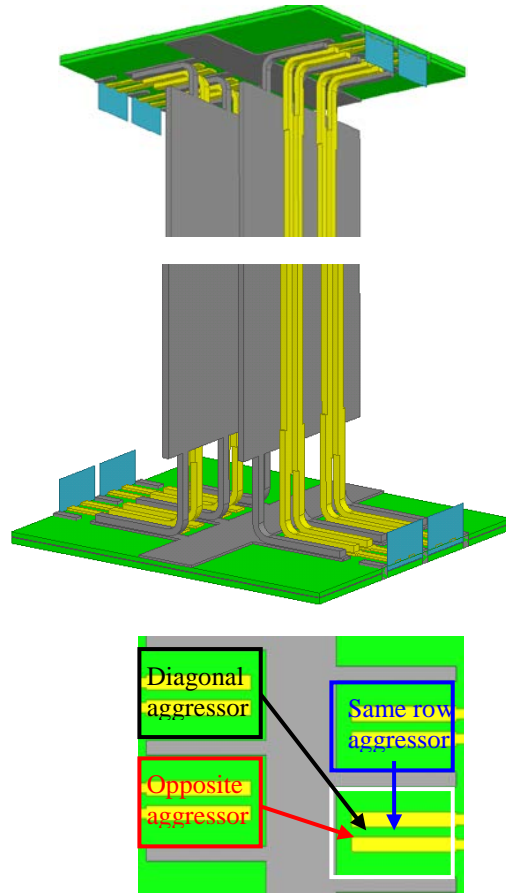


Figure 16. IT9-38H connector with GSSG pin assignment.

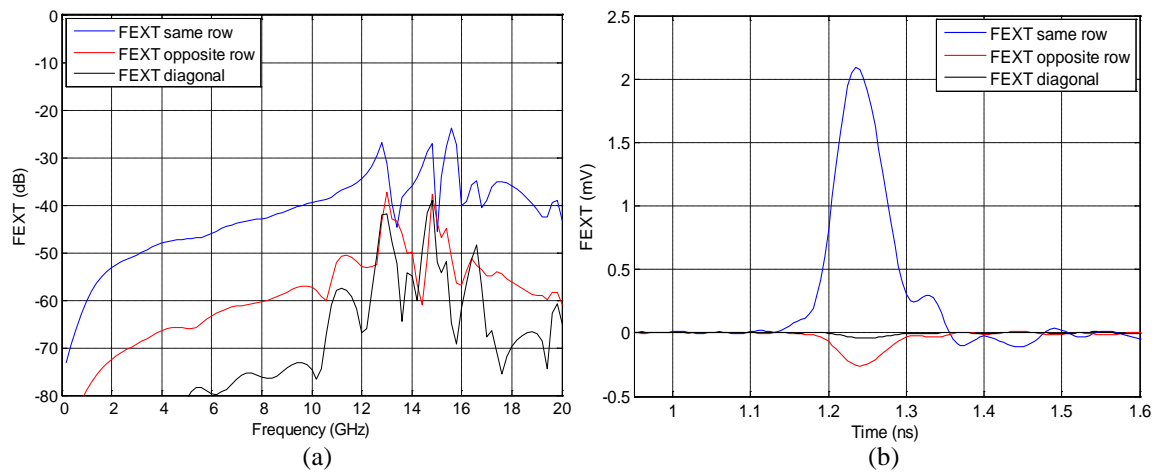


Figure 17. Simulated differential FEXT of IT9-38H connector in frequency and time domains.

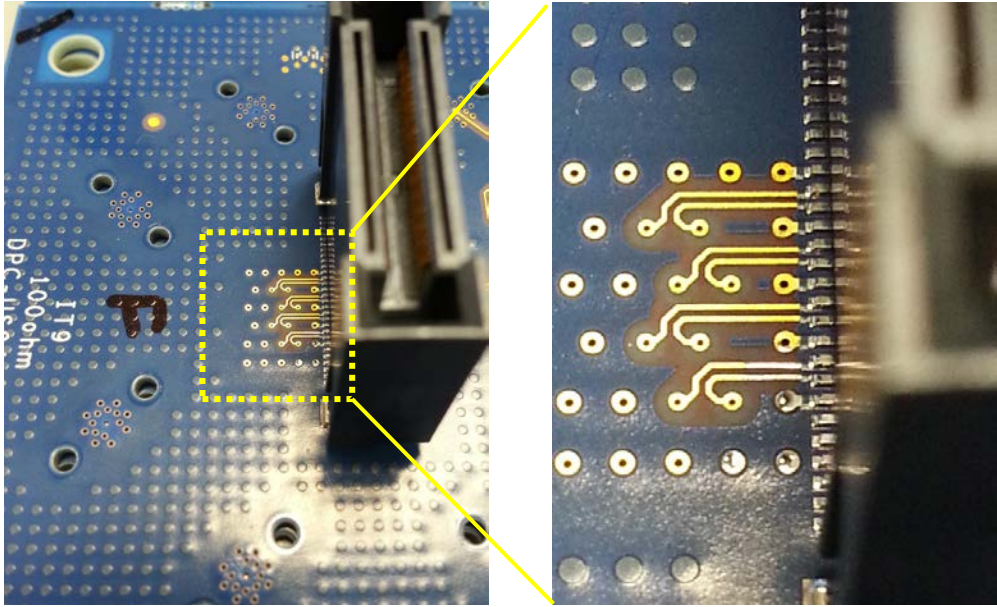
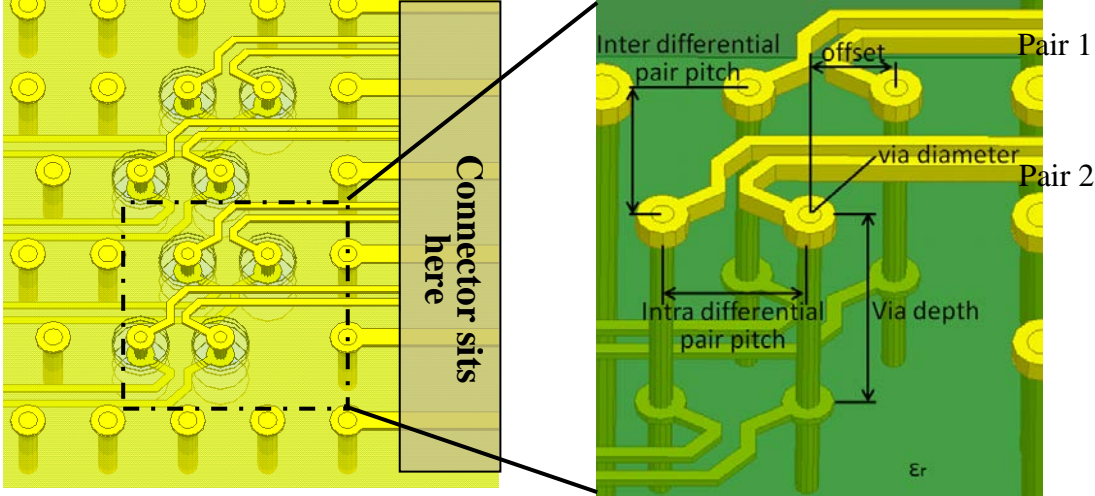


Figure 18. Optimized via design for IT9-38H connector.

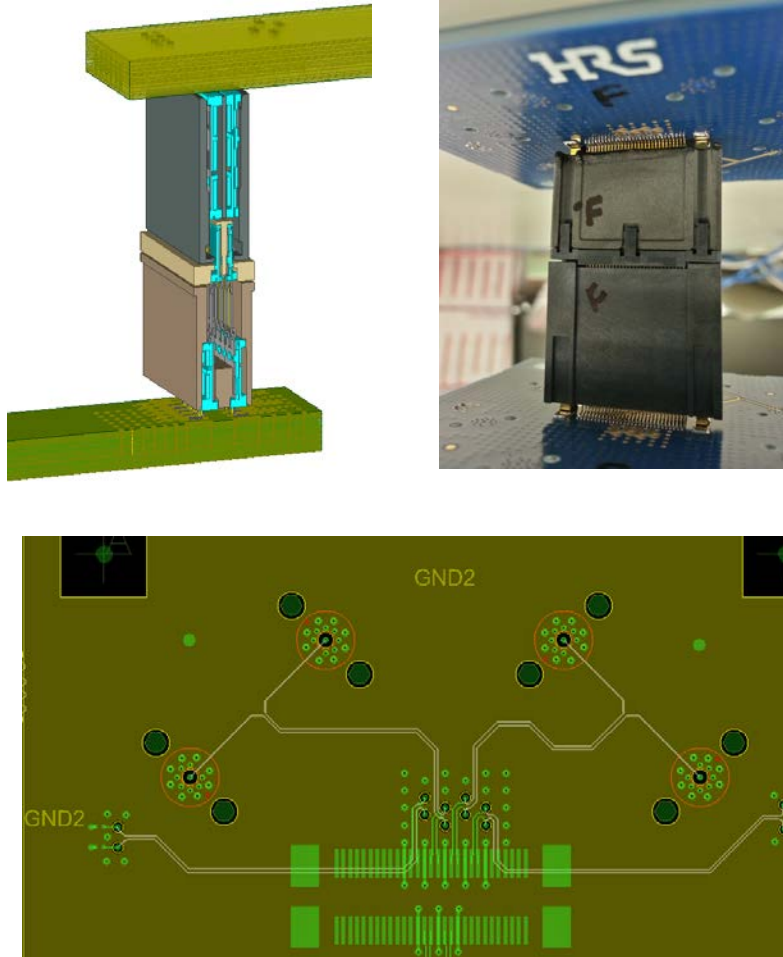
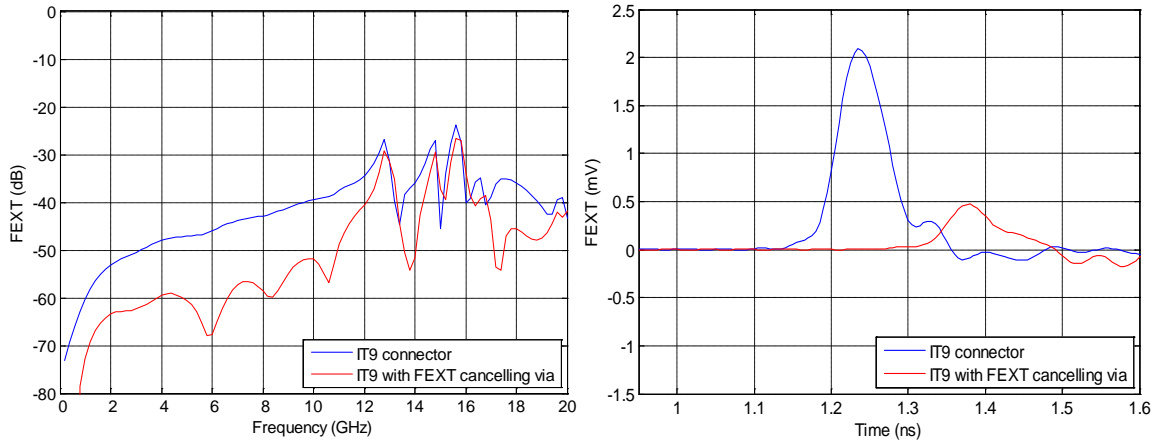
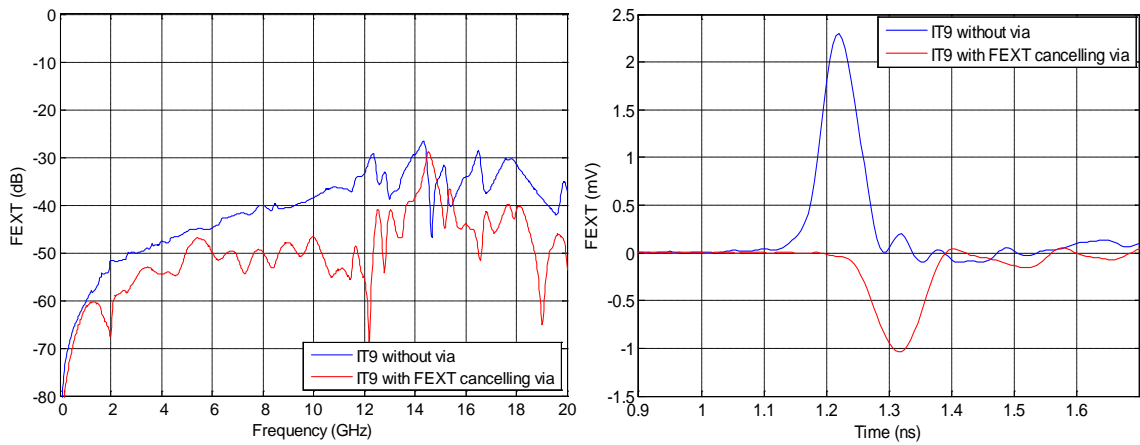


Figure 19. Board assembly

The final board assembly is shown in Figure 19 where SMAs and portion of stripline traces are de-embedded by ISD, leaving short trace + via + IT9-38H + via + short trace as DUT. Figure 20 shows the simulated and measured differential FEXT of IT9-38H connector with and without crosstalk-cancelling vias. The time-domain step response was again created with 1 volt input and 50ps rise time (20% to 80%). The total FEXT of via-connector-via transition is noticeably reduced from the connector's only.



(a) Simulation



(b) Measurement

Figure 20. Frequency- and time-domain differential FEXT of IT9-38H connector with and without crosstalk-cancelling vias. (a) Simulation vs. (b) measurement.

Figure 21 shows the simulated vs. measured insertion loss to crosstalk ratio (ICR) of IT9-38H with and without crosstalk-cancelling vias. The nearest 5 FEXT aggressors are included. It is clear that, with crosstalk-cancelling vias, the channel's ICR is greatly increased (by more than 10dB), giving a lot more margin above the 10GBase-KR spec.

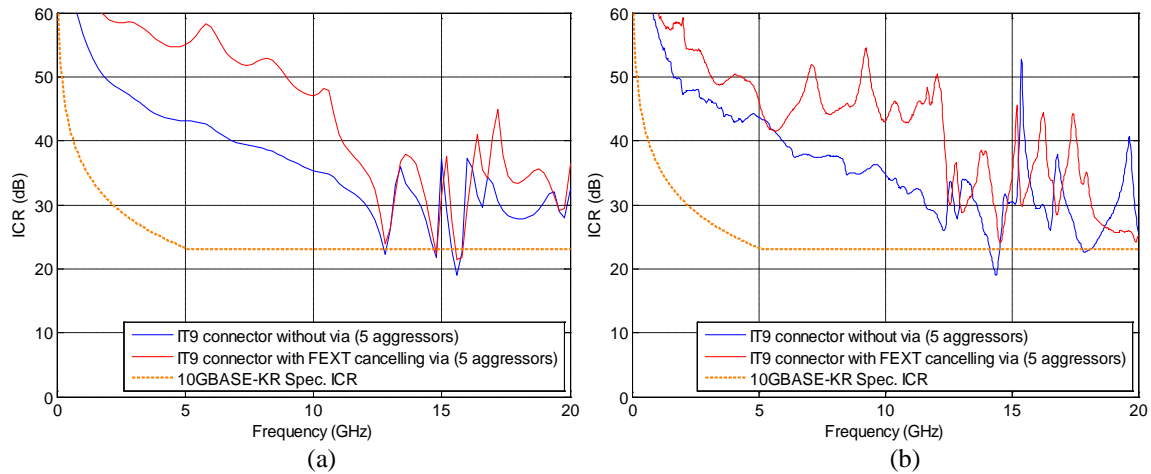


Figure 21. Insertion loss to crosstalk ratio (ICR) of IT9-38H with and without optimized vias. (a) Simulation vs. (b) measurement.

4. Conclusion

This paper presents a new technique to minimize differential crosstalk by adjusting its four single-ended terms. This adjustment can be achieved by simply re-arranging the relative location of signal conductors such that the four single-ended crosstalk terms either cancel each other within an electrical component or give opposite polarities in differential crosstalk among several electrical components in a channel.

There were several myths about differential crosstalk:

1. In a broadside-coupled with offset configuration, a larger offset always gives smaller crosstalk.
2. The crosstalk of via-connector-via transition is larger than the crosstalk of connector itself.

To dispel the myths, test vehicles were built, measured and correlated with simulation. This paper shows that:

1. In a broadside-coupled with offset configuration, there exists an optimal offset that gives minimum crosstalk.
2. With proper via design, the crosstalk of via-connector-via transition can be made less than the crosstalk of connector itself.

The above was easily explained by looking into the makeup and polarity of differential crosstalk. Because FEXT accumulates at the same time at the receiver, pairing a connector with vias that give FEXT of opposite polarity results in reduced FEXT.

The techniques presented in this paper can be applied to design packages, connectors, vias and traces for minimal crosstalk by themselves or to properly layout vias and traces for minimal crosstalk in an entire channel.

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