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Aristotle: A fully automated SI platform for PCB material characterization

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Abstract

This paper introduces a new methodology that extracts PCB material property (DK, DF and surface roughness) by matching all IL, RL, NEXT, FEXT and TDR/TDT of 4-port differential traces. The created models can be used for what-if analysis with width/spacing/thickness variation. Little attention was given to FEXT in the past. This paper shows that both magnitude and phase of FEXT have significant impact on the extracted DK values. The new methodology presented in this paper, from de-embedding to material property extraction to width-, spacing-, length- and frequency-scalable model generation, has been automated in a platform called "Aristotle". This platform helps eliminate human errors in processing voluminous data and provide accurate material information for better PCB design and manufacturing.

Author's Biographies

Jayaprakash Balachandran (JP) is with Unified Compute Server (UCS) Group at Cisco Systems Inc. JP has over 15 years of experience in high speed design and has a PhD in High Speed Interconnects from IMEC Belgium. He has many peer reviewed publications and has been an invited speaker in conferences.

Kevin Cai received the Ph.D. degree in electrical engineering from the University of Ottawa, Ottawa, ON, Canada. He has been a high speed signal integrity engineer assuming different responsibilities for the following companies: Nortel Networks, Sun Microsystems, Juniper Networks, Rambus, and Cisco Systems.

Yang Sun is an engineering manager at Cisco. He joined Cisco in 2009. His team is responsible for hardware design of Cisco's blade server and rack server. He has been focusing on the design with the Intel's latest generation Xeon CPUs. Prior to 2009 he worked in the areas of Optical Transport Network and Packet Transport Network systems design.

Rudong Shi is a senior engineer responsible for hardware design of Cisco's blade and rack server products.

Gene Zhang received the Ph.D. degree in electrical engineering from the University of Beijing, China. He is currently a signal integrity engineer with Unified Compute Server Group at Cisco and is responsible for design of high speed IO links.

Ching-Chao Huang, founder and president of AtaiTec Corporation, has more than 30 years of high-speed design and SI software development experience. He was advisory engineer at IBM, R&D manager at TMA, SI manager at Rambus, and Sr. VP at Optimal. Dr. Huang is an IEEE senior member and he pioneered In-Situ De-embedding (ISD) for causal and accurate de-embedding. He received his BSEE from National Taiwan University and MSEE and PhD from Ohio State University.

Bidyut Sen is a Principal Engineer with Unified Compute Server (UCS) Group at Cisco Systems inc. Bidyut has many years of experience in the computer industry and worked in several companies including Sun Microsystems, Fujitsu and LSI Logic. He has a Ph.D. in Physics from SUNY at Stony brook. Bidyut has several publications, presentations and Patents.

1. Introduction

As SERDES dominates chip IO and data rates continue increasing unabated, the performance of PCB interconnects has become more critical for SERDES link operation than ever before. This PCB interconnect performance largely depends on the dielectric material used. In order to appropriately select the right material for a given application, prospective PCB materials need to be well characterized and understood. There are several parameters of interest for characterization: differential insertion loss per inch, differential impedance, intra-pair timing skew, dielectric constant (DK) and loss tangent (DF). There are, however, three main challenges for characterization: (1) accurate de-embedding of actual fixture being tested, (2) accurate PCB material property extraction to match measurements and (3) the sheer volume of data to be analyzed. To address the above challenges, we developed a set of methodologies and tool framework called "Aristotle". We characterize the PCB interconnects using VNA measurements and de-embed test fixture response using In-Situ De-embedding (ISD) [1-2]. The Aristotle tool framework automates analysis of 100s of S-parameter measurements and generates a comprehensive pdf report that includes (1) S-parameter and TDR/TDT graphs before and after de-embedding, (2) extracted DK, DF and roughness and (3) simulated vs. measured S-parameters and TDR/TDT, etc.

Aristotle uses a new methodology that extracts PCB material property (DK, DF and surface roughness) by matching all IL, RL, NEXT, FEXT and TDR/TDT of 4-port differential traces. The created models are used for what-if analysis with width/spacing/thickness variation. Scalable W-element and S-parameter models are generated for channel simulation.

Several new findings are presented in the following sections. Little attention was given to FEXT in the past. This paper shows that both magnitude and phase of FEXT have significant impact on the extracted DK values. The traditional approach of using a two-layer model with similar core and pre-preg DKs to tune width/spacing and compute impedance does not provide enough accuracy.

2. PCB Material Characterization Overview

Figure 1 shows a generic PCB material characterization flow. The first step is to design test structures for characterization. There are two types of test structures possible depending on how the device under test (DUT) is accessed by the test instrument (Figure 2). Microwave probe based test structures are the simplest to design but measurements with microwave probes can be time consuming. Furthermore, probe measurements tend to have poor repeatability. Another approach is to use SMA or K connectors. These connectorized measurements are highly repeatable, robust and easier to implement. For this reason, we use K connector for this work. However, one of the disadvantages of using SMA or K connectors is that it will be laborious to screw the connectors especially when there are a large number of test structures. For this reason, we experimented with mini-SMP connectors which are 'press on' type and much easier to use. However, we found that the bandwidth of the mini-SMP connector is limited compared to K

connectors. Nevertheless, there are several newer press-on type connectors emerging with better bandwidth characteristics which we plan to use in the future.

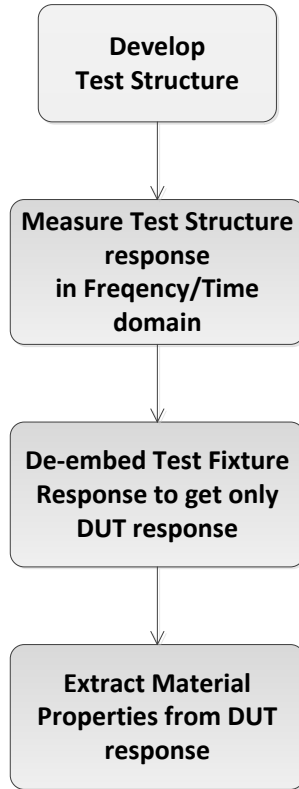


Figure 1. PCB Material Characterization Flow.



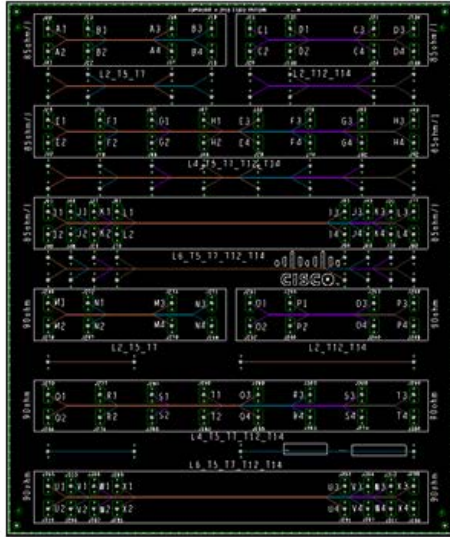
Figure 2. Test structures commonly used for PCB interconnect characterization.

One of the challenges we often encountered is that material data characterized by the fab vendor differ significantly from the response observed in the target application board. These characteristics also vary considerably from one fab vendor to another. It is worth noting that the PCB material characteristics depends not just on the raw material characteristics alone but also on the trace width, spacing and other parameters defined in the PCB stackup (e.g., dielectric resin content and number of plies used). For accurate results, we characterize the PCB interconnects on a characterization platform whose stackup is the same as that of target application board. Figure 3 shows our representative

characterization board templates where the PCB on the left is a dedicated characterization board using K connectors and the PCB on the right, which uses mini-SMP connectors, can be piggy backed on the target application board.

The PCB interconnect characterization can be done in time or frequency domain. The time-domain characterization can be done using TDR/TDT measurements with low cost test instruments. SET2DIL [3] is one of the popular methods that use time-domain

Characterization PCB Template



Coupon Template

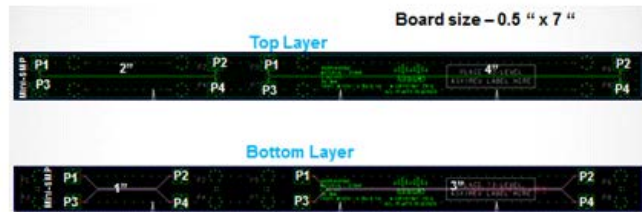


Figure 3. PCB Characterization board Templates.

characterization but it is limited to characterizing only insertion loss. The challenges with time-domain measurements are (1) accurate calibration of test instrument to the measurement point and (2) the limited dynamic range for wide bandwidth of frequencies. For these reasons, we use VNA based 4-port frequency-domain measurements which inherently enable wide bandwidth characterization. The calibration is also simple and straightforward with Electronic Calibration modules.

The next set of challenges in characterization arise from de-embedding of test fixture response to get DUT only response. The test fixture in this work refers to SMA or K connector and a lead-in trace (Figure 4). There exist several de-embedding methods. TRL (thru-reflect-line) calibration [4] is one popular technique used in microwave circuits. However, TRL requires that multiple test coupons be built and measured. In addition, TRL is prone to causality error [1]. There are other methods such as ISD [1-2], AFR[5] and GMS [6-7] that require only two line standards, a long and short line. For this work, we use ISD to first de-embed the DUT response. Then, we extract material and other parameters of interest from the DUT response by matching measured and simulated IL, RL, NEXT, FEXT and TDR/TDT as outlined Figure 1. We chose ISD after rigorous evaluation of several test cases including the test cases defined in IEEE P370 working group [8]. Figure 5 shows an example from IEEE P370 working group where a 45 ohm

2x thru (M11) is used to de-embed 50 ohm fixture exp 3.1.1 in the test structures M16 and M18. Note that M11, M18 and M19 test structures are defined such that DUTs exp. 4.1.1 and exp. 4.3.9 can be individually measured and compared with the de-embedded results. Figure 6 and Figure 7 compare the DUT results extracted by ISD vs. an alternate method ("Split 2x thru") that uses one half of 2x thru directly for de-embedding. Artificial ripples caused by non-causality in "Split 2x thru" results can be clearly seen. On the other hand, the ISD extracted results are shown to be causal and they match the original data quite well even when the 2x thru and fixture impedance differ by more than 10%. More details of the de-embedding method in ISD are described in Section 4.

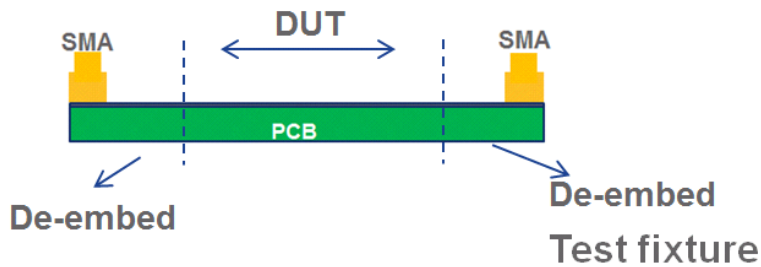


Figure 4. DUT and Test fixture in a typical PCB interconnect test structure.



Figure 5. Using 45 ohm 2x thru to de-embed 50 ohm fixtures.

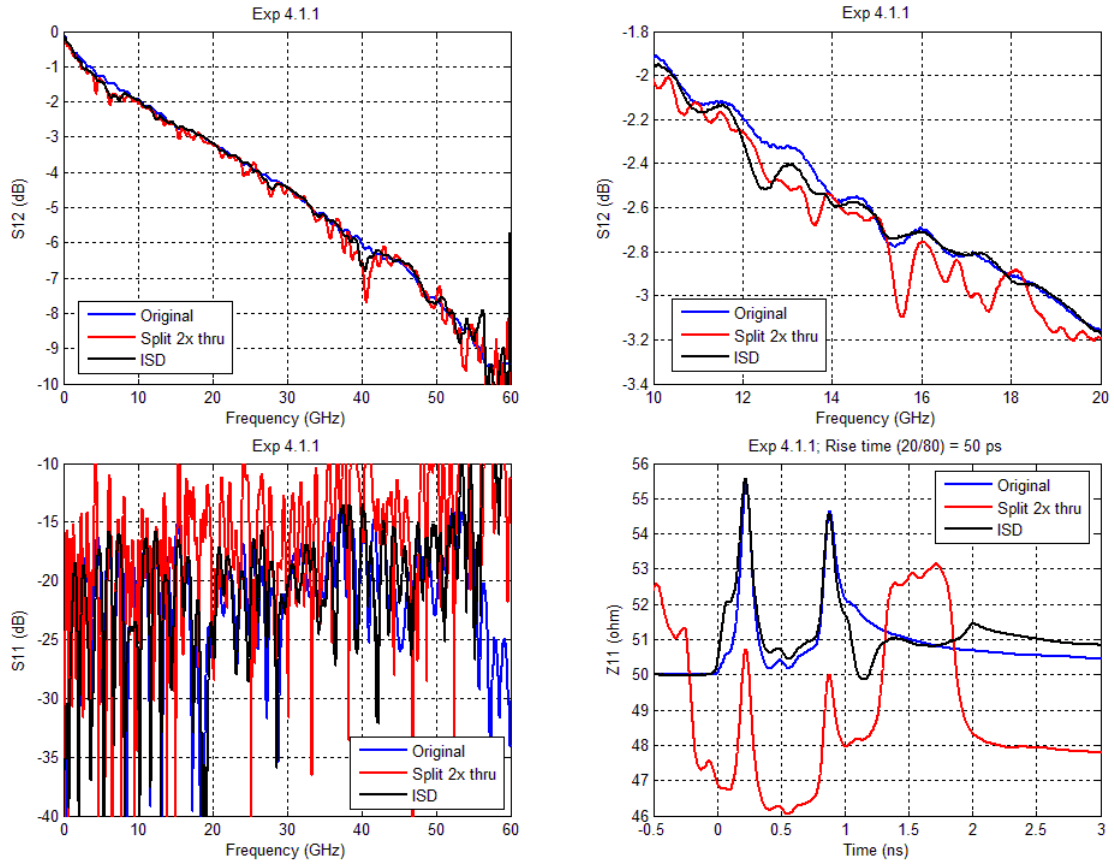


Figure 6. Extracted DUT (Exp 4.1.1 microstrip in Figure 5) results.

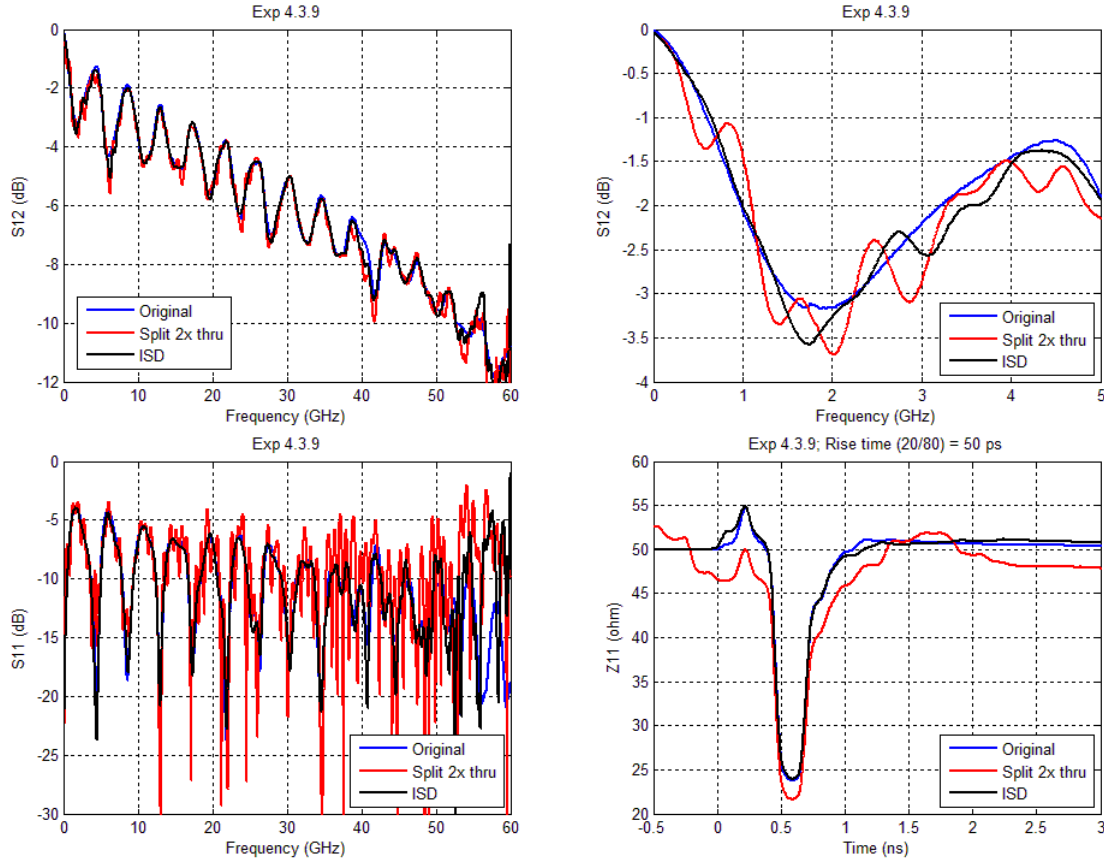


Figure 7. Extracted DUT (Exp 4.3.9 Beatty standard in Figure 5) results.

3. Automation Flow

Figure 8 shows the automation flow used in this work. Aristotle reads a control file in Excel format and processes the S-parameter files as directed in the control file. It then generates material characterization report in pdf format, stores de-embedded S-parameter files in Touchstone format and extracts material characteristics for scalable W-element and S-parameter model generation. The pdf report includes a summary of material characteristics containing loss per length, intra-pair timing skew, dielectric constant (DK) and loss tangent (DF). In addition, the report includes insertion loss, return loss, TDR plots of the test structures, and PCB stackup and transmission line cross sections if available. Figure 9 shows a representative control file. As can be seen from the control file, the stackup, differential pair width/spacing (W/S) and PCB layout views are captured as image files for inclusion in the report file. Current implementation allows for transmission lines with up to 4 different lengths (L2, L3, L5, and L7) and up to 3 de-embedding combinations. The de-embedding combination specifies long and short lines to be used to extract DUT response. Although one de-embedding combination is sufficient, additional de-embedding combinations help enhance the accuracy of data collected through averaging. It also helps us understand any variation in the data

extracted. There can be up to 3 W/S for a given differential pair impedance. This allows for instance to study insertion loss impact as W/S changes and helps to optimize it. Line 23 in Figure 9 specifies the differential pair impedance for which it is designed for. This impedance value will be used to re-normalize the impedance of measured S-parameters if the test structure differential impedance is not 100 ohms. The renormalization is done to remove ripples from insertion loss and give true attenuation at any given frequency. Frequencies at which loss per inch is desired can also be specified. Usually, these frequencies specified correspond to the Nyquist frequency of different IO standards such as PCIe Gen 4 and 100GbE. The insertion loss per inch reported in the form of a table at specified frequencies for all the layers characterized. For TDR plots, rise time for which TDR waveform is calculated is specified (Line no. 24).

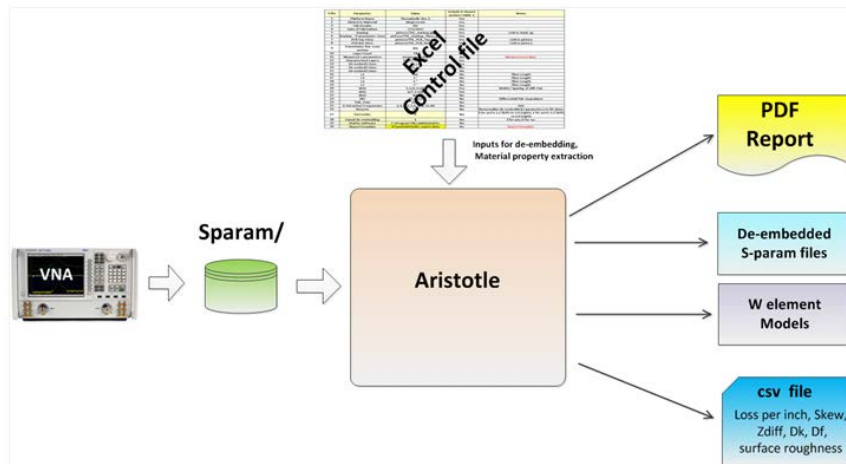


Figure 8. Automation flow for PCB material characterization.

S.No	Parameter	Value	Include in Report section I Table 1	Notes
1	Platform Name	MyTestBoard Rev 1	Yes	
2	Dielectric Material	xxxx	Yes	
3	Fab Vendor	xxxx	Yes	
4	Date of Fabrication	1/10/2016	Yes	
5	Stackup	picture/THL_stackup.jpg	Yes	Link to stack up
6	Stackup - Transmission Lines	picture/THL_stackup_Tlines.jpg	Yes	
7	PCB Top View	picture/THL_PCB_Top.jpg	Yes	Link to picture
8	PCB Bot View	picture/THL_PCB_Bot.jpg	Yes	Link to picture
9	Transmission line cross section	NA	Yes	
10	Layer Count	18	Yes	
11	Measured s-parameters	measurements/	No	
12	Characterized Layers	T5, T7, T10, T12, T14	Yes	
13	De-embed1 Lines	L3, L7	Yes	
14	De-embed2 Lines	L5, L7	Yes	
15	De-embed3 Lines	NA	No	
16	L2	NA	No	Tline Length
17	L3	3 "	No	Tline Length
18	L5	5 "	No	Tline Length
19	L7	7 "	No	Tline Length
20	WS1	5.2/6.3 mils	Yes	Width / Spacing of diff. Pair
21	WS2	6/7.2 mils	Yes	
22	WS3	NA	No	
23	Z85	85 ohms	No	Differential Pair Impedance
24	TDR_Trise	35 ps	No	
25	IL Extraction Frequencies	3, 4, 5.2, 5.6, 6, 8, 12.89	No	GHz
26	Renorm	ON	No	Renormalize de-embedded s-parameters to 85 ohms
27	Port order	2	No	
28	AtaITec software	C:\Program Files (x86)\AtaITec	No	
29	Report template	ISD_report.dotx	No	

Figure 9. Aristotle control file in Excel format.

4. Material Property Extraction Algorithms

Causal de-embedding

Accurate de-embedding is crucial for material property extraction. Consider Figure 10 where a DUT is mounted on a fixture and, in traditional approach, data from separate test coupons are used directly for de-embedding. Due to difference in fiber weave, etching, routing, soldering and connectors, however, the fixture and test coupons are never identical. The difference between fixture and test coupons, mainly in the form of impedance, is like “phantom limbs” [9] that contribute to non-causal S parameters after de-embedding. Such non-causality makes simulation vs. measurement correlation impossible. Figure 11 shows the de-embedding flows of In-Situ De-embedding (ISD) [1-2] vs. "Split 2x thru". Instead of splitting 2x thru test coupons directly, ISD adjusts 2x thru or 1x open/short data for de-embedding through a numerical optimizer to match the fixture's TDR impedance. As a result, the extracted DUT's S parameters are causal and there is no need to tighten the impedance variation between fixture and test coupons, reducing hardware cost.

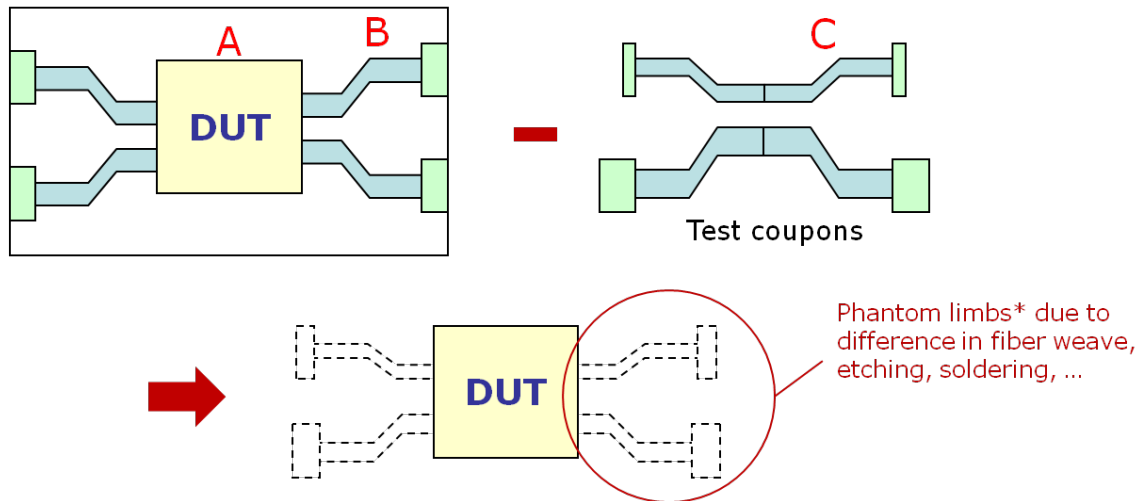


Figure 10. Difference between test coupons and fixture can result in causality error in traditional de-embedding.

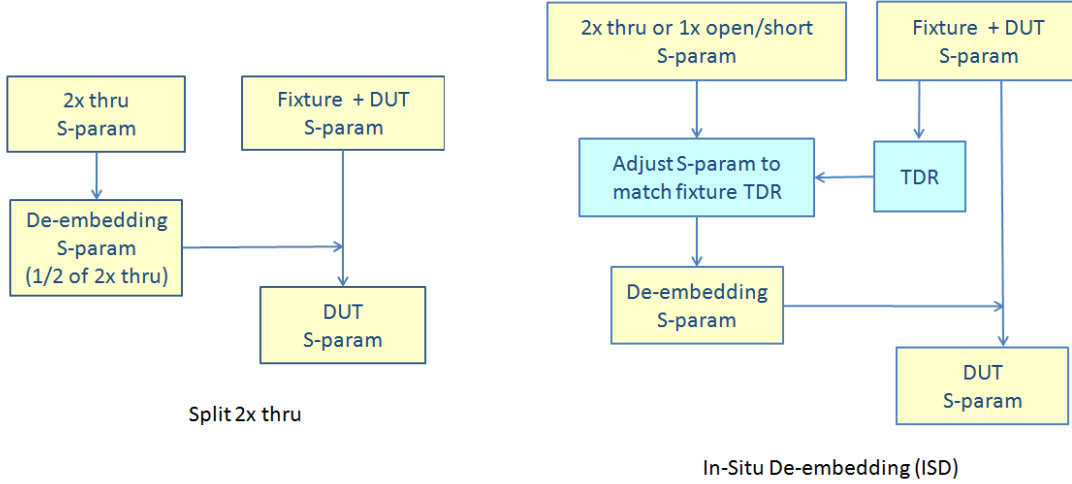


Figure 11. De-embedding flows of ISD vs. "Split 2x thru" method.

Fitted model

The de-embedding yields 4-port S-parameters of the differential-pair traces referred to as DUT in Figure 4. This de-embedded 4-port S-parameters are fitted to match with a 2D field solver model. The 2D field solver can use one of five dielectric constructions shown in Figure 12. Note that the dielectric constructions can vary even for a given dielectric based on a number of factors such as process, weave type and number of plies. Key parameters such as trace width, spacing between traces, DK, DF, surface roughness and effective conductivity are optimized within user-defined tolerance values to achieve good correlation between the 2D field solver model and de-embedded trace-only S-parameters. This optimization for model fitting is done without any user intervention.

The roughness of each matte- and drum-side surface of signal and ground metals (R1 to R5 in Figure 12) is modeled by effective conductivity [10]. The derived frequency-dependent conductivity (i.e., effective conductivity) can be conveniently entered in a table into a commercial field solver (such as HFSS) to account for additional loss at high frequencies and its effect on all IL, RL, NEXT and FEXT.

The dielectric constant (DK) and dissipation factor (DF) of each layer are modeled by the causal Djordjevic-Sarkar equation [11]:

$$\begin{aligned}\varepsilon &= \varepsilon_{\infty} + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10} \left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f} \right) \\ &= \varepsilon_r \cdot (1 - i \cdot \tan \delta)\end{aligned}\tag{Eq. 1}$$

where ε_r is DK, $\tan \delta$ is DF and f is frequency in Hz.

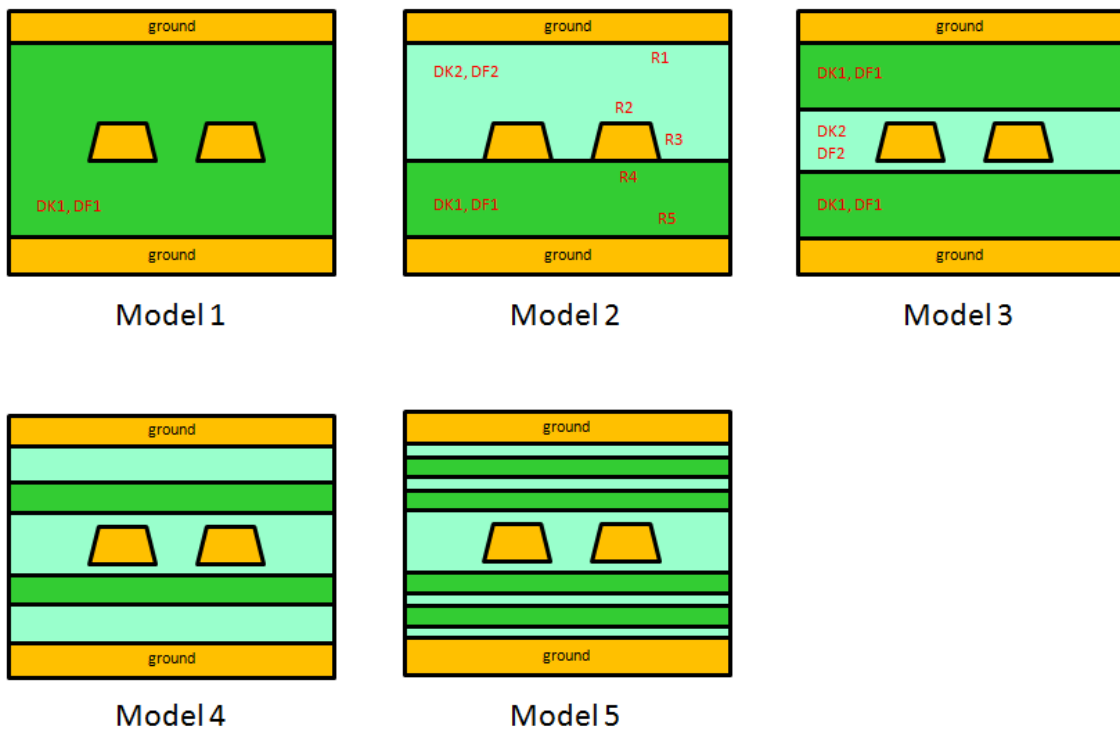


Figure 12. Cross-sectional geometries used for material property extraction where DK1, DF1, DK2, DF2 and roughness (R1 to R5) are to be extracted.

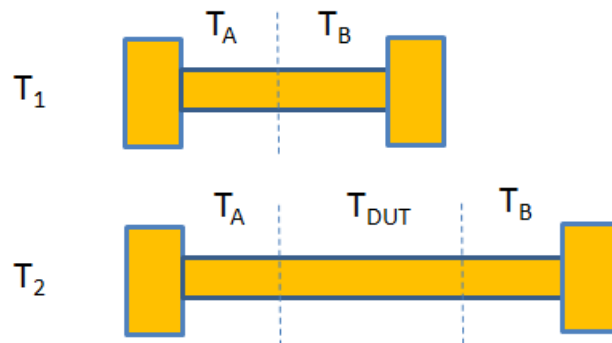


Figure 13. Computing T_{DUT} from T matrices of two trace structures (T_1 and T_2).

5. Results

Extracting attenuation

Consider Figure 13 where measured S parameters of two different trace lengths are converted into T matrices (T_1 and T_2) first. Each 2-port S to T conversion can be computed by

$$\begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = \frac{1}{S_{21}} \begin{pmatrix} S_{12}S_{21} - S_{11}S_{22} & S_{11} \\ -S_{22} & 1 \end{pmatrix} \quad \text{Eq. 2}$$

For the short trace:

$$T_1 = T_A \cdot T_B \quad \text{Eq. 3}$$

and for the long trace:

$$T_2 = T_A \cdot T_{DUT} \cdot T_B \quad \text{Eq. 4}$$

where T_A , T_B and T_{DUT} are the T matrices of left fixture, right fixture and DUT, respectively. It has been assumed that the short and long trace structures (T_1 and T_2) have identical fixtures (T_A and T_B). Then [12-14],

$$T_2 \cdot T_1^{-1} = T_A \cdot T_{DUT} \cdot T_A^{-1} \quad \text{Eq. 5}$$

For a transmission line, T_{DUT} can be diagonalized and written as:

$$T_{DUT} = P \cdot \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{pmatrix} \cdot P^{-1} \quad \text{Eq. 6}$$

Apparently the eigenvalues ($e^{\pm\gamma l}$) of T_{DUT} and $T_2 T_1^{-1}$ are the same.

Let

$$T_2 \cdot T_1^{-1} = \begin{pmatrix} a & b \\ c & d \end{pmatrix} \quad \text{Eq. 7}$$

then

$$e^{-\gamma l} = \frac{(a+d) \pm \sqrt{(a-d)^2 + 4bc}}{2} \quad \text{Eq. 8}$$

Consider an example where the differential insertion loss (SDD12) of 2" traces is extracted from 5" and 7" trace structures (L5 and L7) in Layer 5 of Figure 3. Comparison of ISD result vs. eigenvalue ($e^{-\gamma l}$) is shown in Figure 14. The ISD result is normalized to 90 ohm reference impedance. Glitches and ripples from the eigenvalue solution are seen, which are due in part to the difference between fixtures of L5 and L7 and in part to the

assumption of uniform transmission line. Proper root tracking using data from multiple lines may help remove some glitches [15].

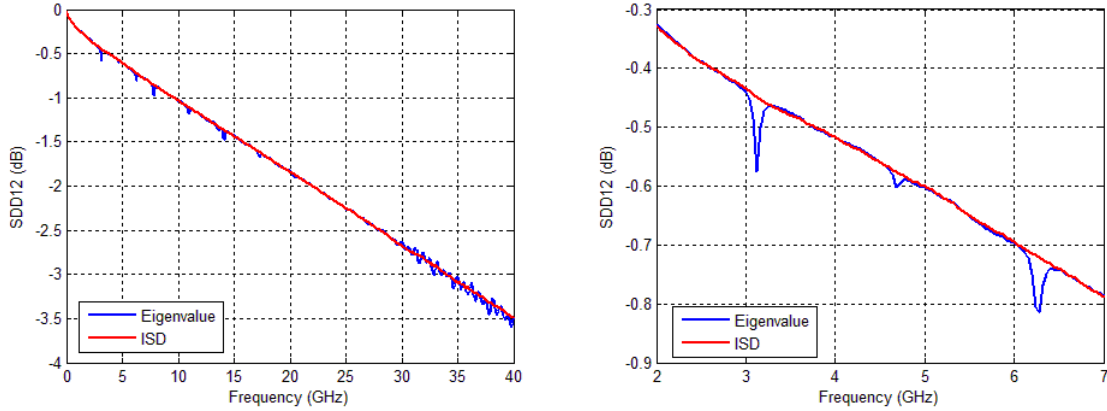


Figure 14. Differential insertion loss (SDD12) of 2" traces extracted by ISD vs. attenuation calculated by eigenvalue.

The insertion loss per inch is extracted from the de-embedded trace S-parameters at user-defined frequencies and is tabulated for easy reading. Table 1 shows the tabulated insertion loss per inch for the PCB shown in Figure 3.

Freq	Layer 3	Layer 5	Layer 7	Layer 10	Layer 12	Layer 14
GHz	L2L7T3WS1	L2L7T5WS1	L2L7T7WS1	L2L7T10WS1	L2L7T12WS1	L2L7T14WS1
3	-0.200208	-0.214174	-0.23112	-0.230748	-0.210656	-0.198021
4	-0.240618	-0.257358	-0.279482	-0.277466	-0.253062	-0.237836
5.2	-0.290562	-0.309116	-0.334012	-0.337278	-0.304094	-0.285004
5.6	-0.307278	-0.326626	-0.352522	-0.358242	-0.32128	-0.303108
6	-0.324214	-0.345294	-0.371136	-0.37261	-0.33808	-0.32046
8	-0.403222	-0.426578	-0.459442	-0.457102	-0.419742	-0.393126
12.89	-0.59184	-0.623564	-0.67018	-0.665518	-0.612678	-0.573016

Table 1. Insertion loss per inch for various layers of the PCB shown in Figure 3.

Impedance

Due to the fiber weave effect, a PCB trace is not a uniform transmission line. The definition of PCB trace impedance can become ambiguous, considering that it is dependent on location, rise time and attenuation. At the same time, it is desirable to communicate with the PCB vendors using just one simple impedance number that is meaningful for the data rate of interest. This paper proposes the following approach for consistent reading of PCB trace impedance.

Consider Figure 15 where S parameters of PCB trace (after de-embedding) are varied

with reference impedance. The PCB trace impedance is defined by the reference impedance when the reflected energy (φ) is minimized:

$$\varphi = \int_{f_{min}}^{f_{max}} \{|S_{11}(f)|^2 + |S_{22}(f)|^2\} \cdot |w(f)|^2 df \quad \text{Eq. 9}$$

with

$$w(f) = \frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b} \quad \text{Eq. 10}$$

and T_r =rise time (0 to 100%) and T_b =bit time of input trapezoidal pulse.

Figure 16 shows SDD11 and TDR (i.e., ZDD11) of the same de-embedded 2" traces from the previous section with reference of 100 ohm and 89.86 ohm, respectively. The reference of 89.86 ohm was derived from Eq. (9) with $f_{min}=0$, $f_{max}=40$ GHz, $T_r=16$ ps (0 to 100%) and $T_b=40$ ps. The methodology of Eq. (9) helps us identify one number for PCB trace impedance from the varying TDR curve.

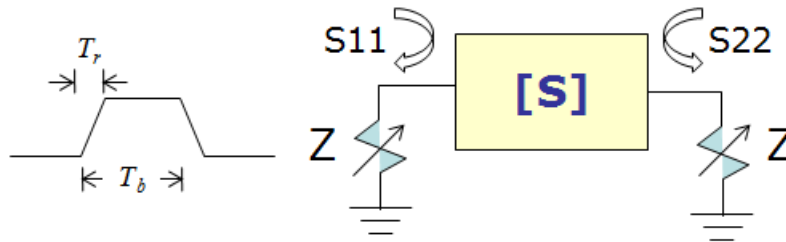


Figure 15. Vary reference impedance for minimal S11 and S22.

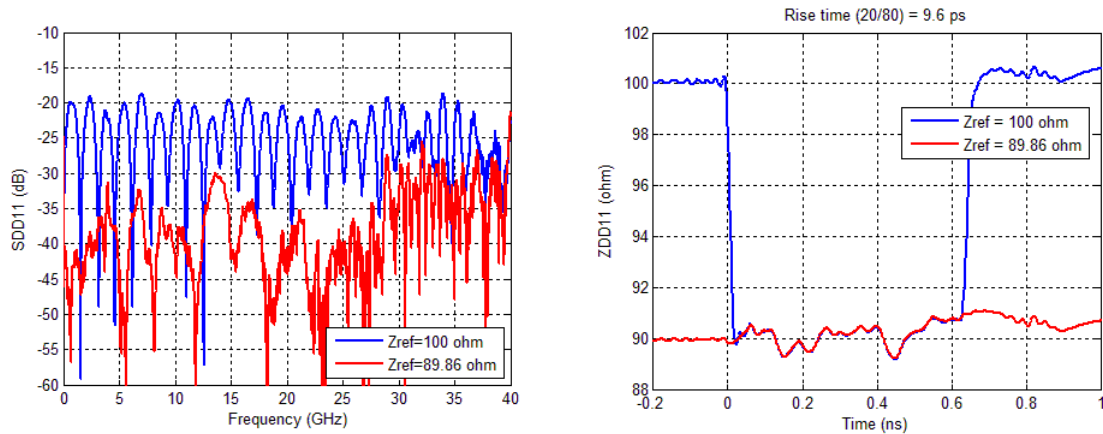


Figure 16. PCB trace impedance is defined by the reference impedance at which Eq. (9) is minimized.

Figure 17 shows impedance extracted as per Eq. (9) for 5" and 7" traces in different layers before and after de-embedding. Note that the trace impedance before de-embedding (L5WS1/L7WS1) is higher than de-embedded trace (ISD) due to 50Ω K-

connector fixture impedance. This impedance plot, generated as part of automated report, helps to instantly grasp the impedance variation of traces in different layers.

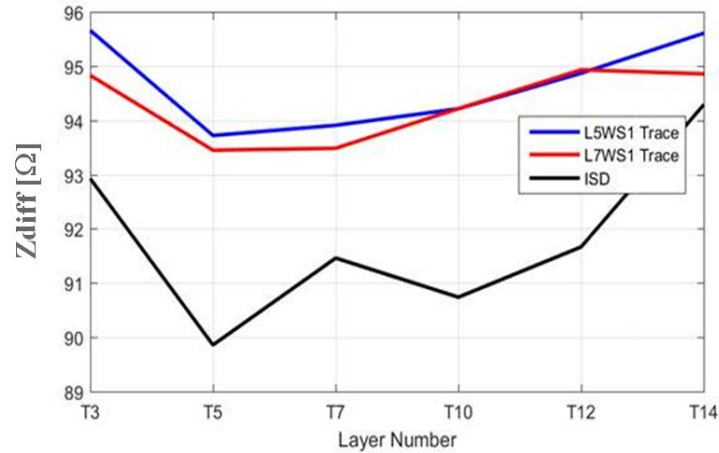


Figure 17. Differential impedance extracted as per Eq. (9) for different layers.

Dielectric DK / DF extraction

Models 1 to 5 of Figure 12 were used to extract DK, DF, roughness and trace width/spacing. Except for Model 1 which cannot correlate FEXT, all other models correlate well in every term with the measured trace response (after de-embedding). Figure 18 to Figure 28 show the measured (after de-embedding) vs. fitted single-ended, differential-mode and common-mode IL, RL, NEXT, FEXT, and TDR/TDT using Model 3. All terms across a wide frequency range are fitted very well. The extracted DK1, DF1 (green layer) of Model 3 are given by:

$$\begin{aligned}\varepsilon_{\infty} &= 3.27929 \\ \Delta\varepsilon &= 0.144348 \\ m1 &= 9.58619 \\ m2 &= 15.4109\end{aligned}$$

and the extracted DK2, DF2 (light blue layer) are given by:

$$\begin{aligned}\varepsilon_{\infty} &= 3.46724 \\ \Delta\varepsilon &= 0.170196 \\ m1 &= 9.58715 \\ m2 &= 14.8352\end{aligned}$$

The extracted surface roughness (Rq) is 0.324321 μm . The corresponding DK, DF and effective conductivity are shown in Figure 29 to Figure 33. For system design, the extracted material models can be used in 2D/3D field solvers for model generation.

Figure 34 to Figure 35 show the measured vs. fitted single-bit response and eye diagram at 25 Gbps and 10 ps rise time (20/80). No equalization was applied. Both eye height (EH) and eye width (EW) for a PRBS12 pattern are found very close: EH=0.904578 volt (measured) vs. 0.91192 (fitted) and EW=39.0764 ps (measured) vs. 39.202 ps (fitted).

Comparison of Models 1 to 5

Models 2 to 5 all give good correlation between simulated and measured IL, RL, NEXT, FEXT and TDR/TDT. Model 1 has only one dielectric so it cannot correlate FEXT. Table 2 compares extracted DK1 and DK2 at 10 GHz for Models 1 to 5. Now a key question is which of these models (2 to 5) is physical. Figure 36 shows the cross section of trace being modeled. As can be seen, the dielectric construction is not uniform and it can vary along the length of trace. This non-uniform dielectric construction would be difficult to model as is. Therefore, Models 2 to 5 can be considered "equivalent". The following observations can be made regarding the physical nature of each model. Model 2 shows large difference in DK1 and DK2 values which is not expected for the material used. Model 4 and 5 show higher DK values than expected. DK1 value from model 3 looks reasonable as compared to fab specified values. However, DK2 value in the middle layer seems higher as the middle layer is expected to be pure resin. The main reason for this higher value of DK is attributed to the 'glass-stop' phenomenon where much of the resin is squeezed out of the prepreg layers that the glass cloth is in contact with (or nearly in contact with) the signal traces. There are also glass bundles seen between the signal traces which tend to increase DK in the middle layer.

The phenomenon of larger DK in the middle layer in this case can also be explained by the time-domain FEXT curve in Figure 26 where the polarity is the same as the input signal's (i.e., FEXT swings positive with a positive input signal). Because FEXT is proportional to $K_C - K_L$ with K_C = capacitive coupling and K_L = inductive coupling, for FEXT to have the same polarity as input signal, K_C must be larger than K_L . For Model 3 in Figure 12, it is inevitable that, in order to have $K_C > K_L$, the middle layer has larger DK than the top and bottom layers. The above finding shows the importance of matching all IL, RL, NEXT and FEXT in both frequency and time domains for material property extraction. Important information can be overlooked if not all terms are matched and correlated.

Model	DK1	DK2
1	3.510	-
2	2.444	4.294
3	3.413	3.623
4	3.863	3.360
5	3.115	3.975

Table 2. Extracted DK1 and DK2 at 10 GHz.

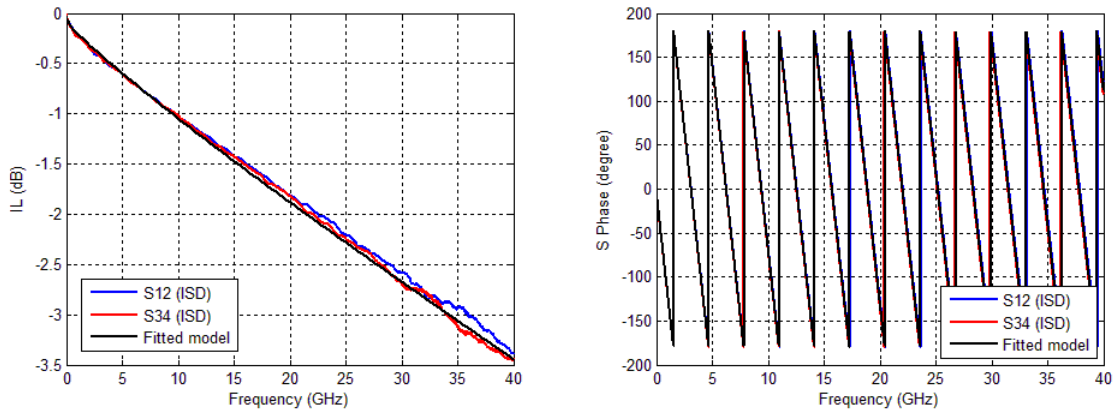


Figure 18. Measured vs. fitted single-ended IL. Magnitude and phase.

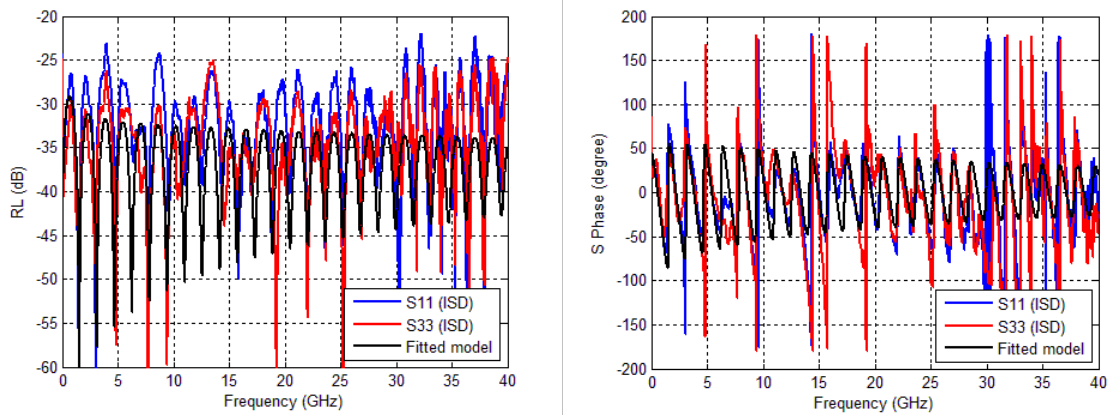


Figure 19. Measured vs. fitted single-ended RL. Magnitude and phase.

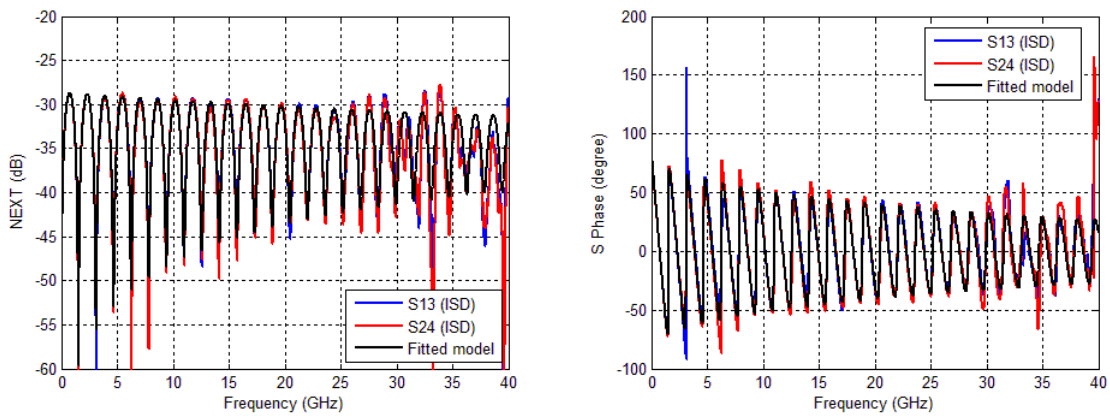


Figure 20. Measured vs. fitted single-ended NEXT. Magnitude and phase.

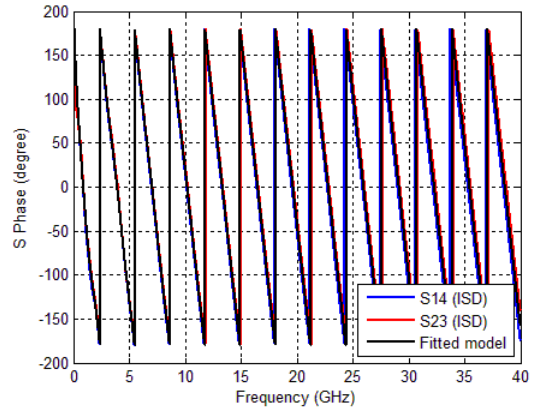
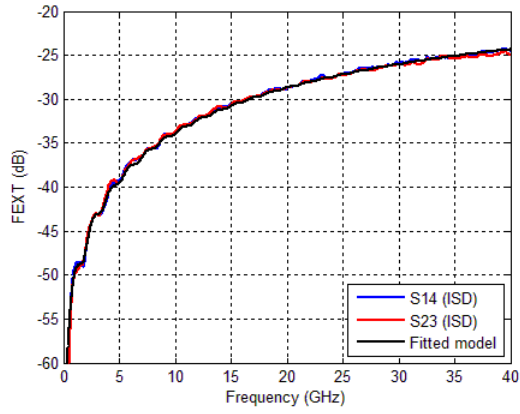


Figure 21. Measured vs. fitted single-ended FEXT. Magnitude and phase.

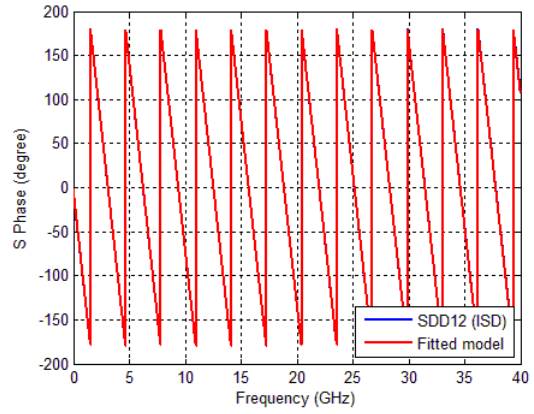
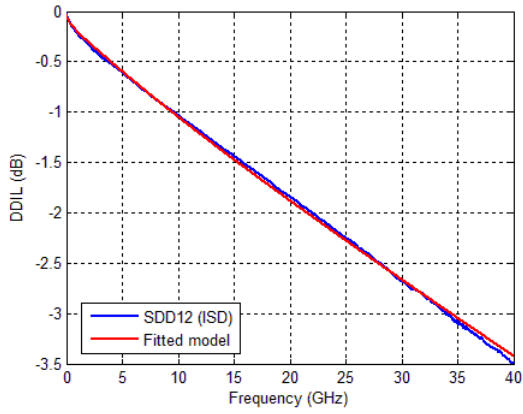


Figure 22. Measured vs. fitted differential IL. Magnitude and phase.

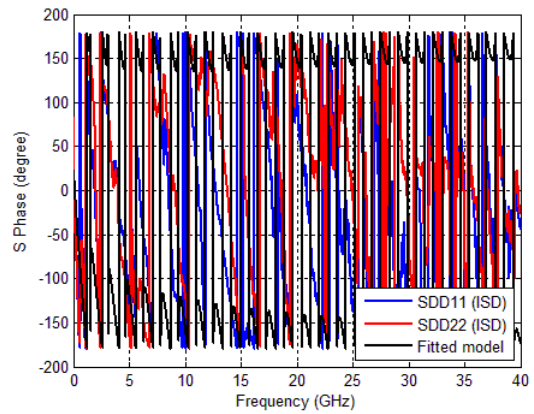
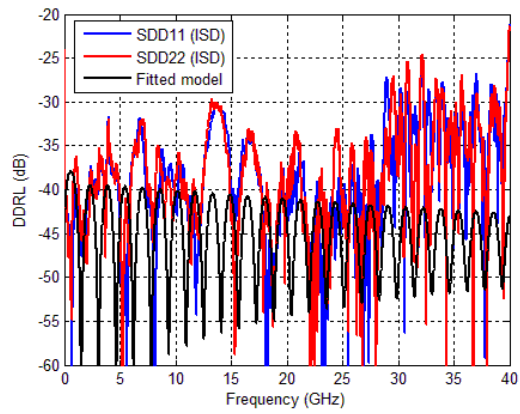


Figure 23. Measured vs. fitted differential RL. Magnitude and phase.

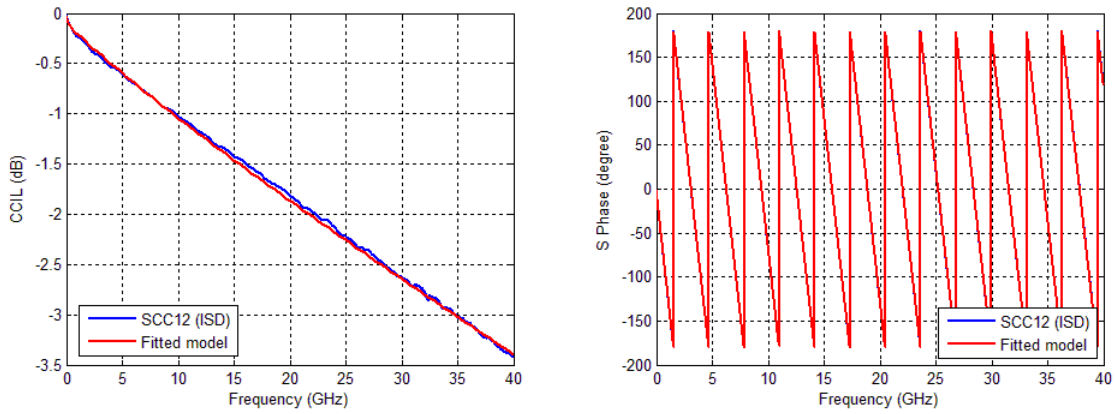


Figure 24. Measured vs. fitted common-mode IL. Magnitude and phase.

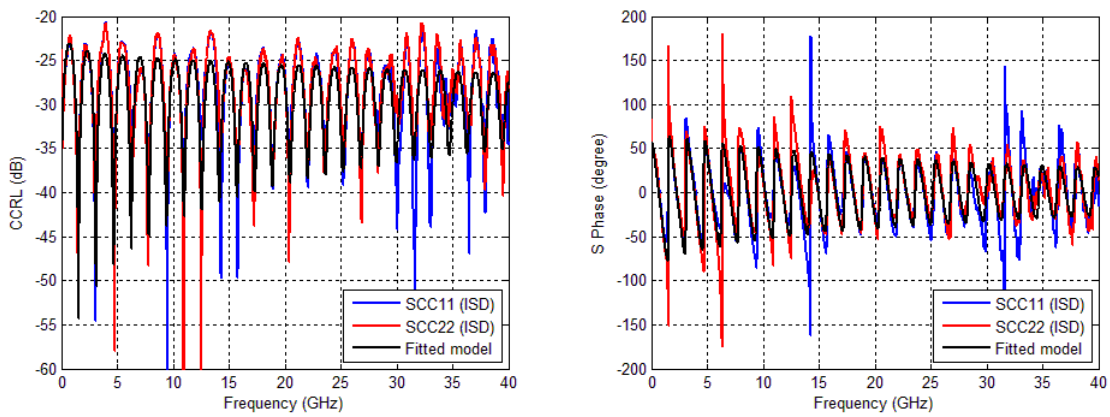


Figure 25. Measured vs. fitted common-mode RL. Magnitude and phase.

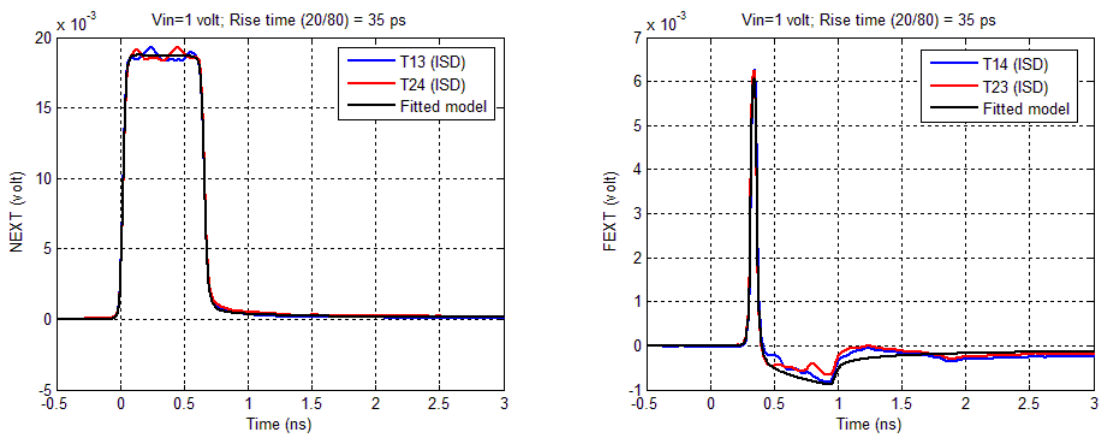


Figure 26. Measured vs. fitted single-ended NEXT and FEXT in time domain.

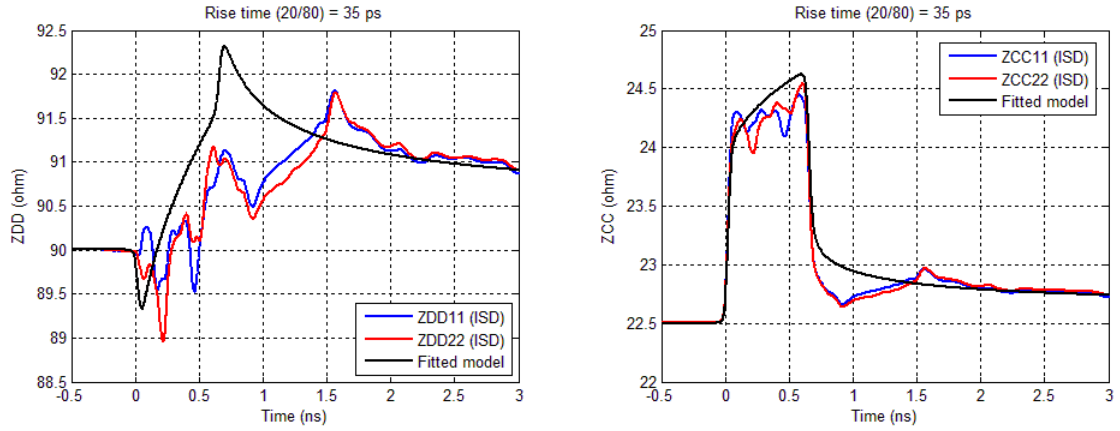


Figure 27. Measured vs. fitted differential- and common-mode impedance.

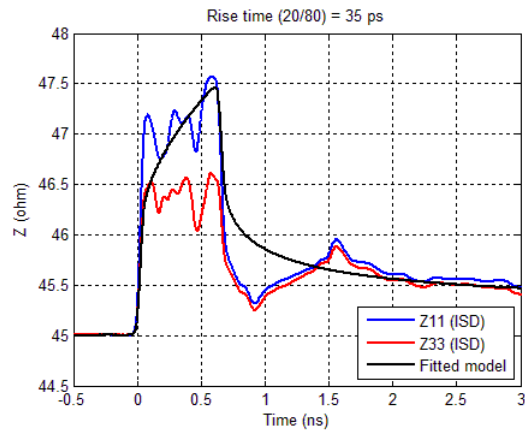


Figure 28. Measured vs. fitted single-ended impedance.

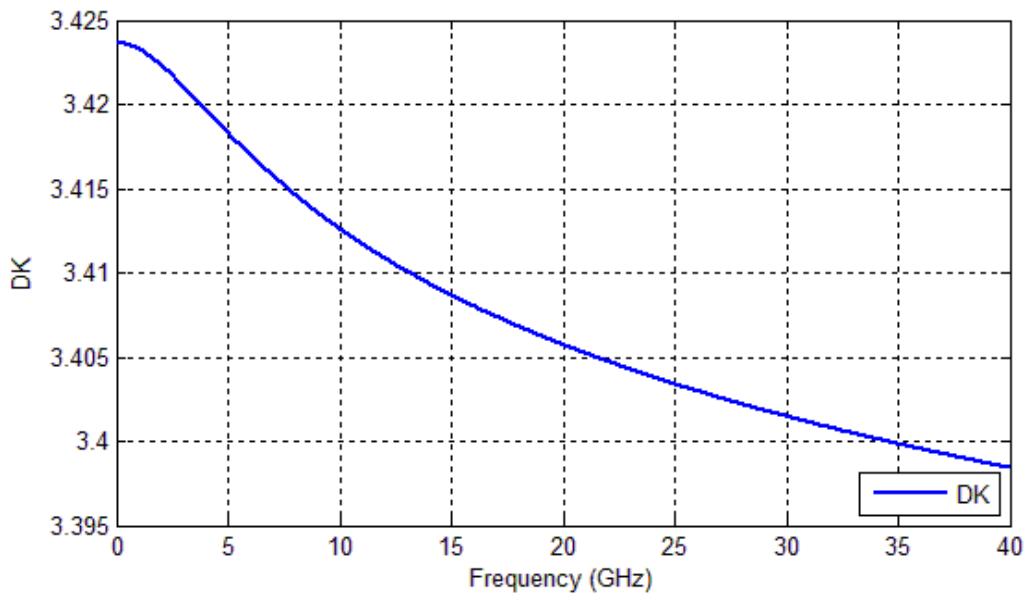


Figure 29. Extracted DK1 (green layer).

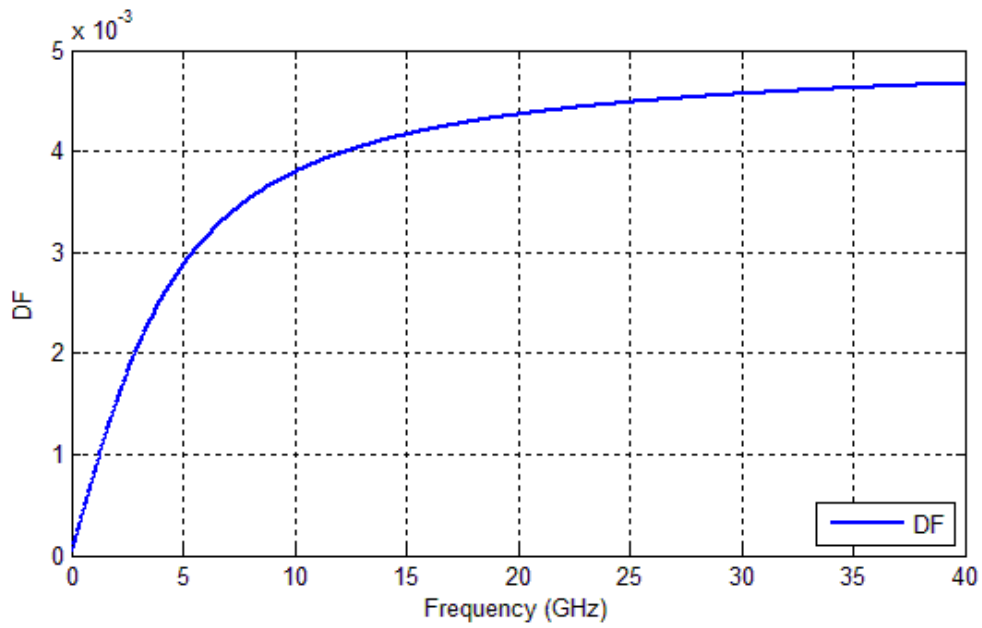


Figure 30. Extracted DF1 (green layer).

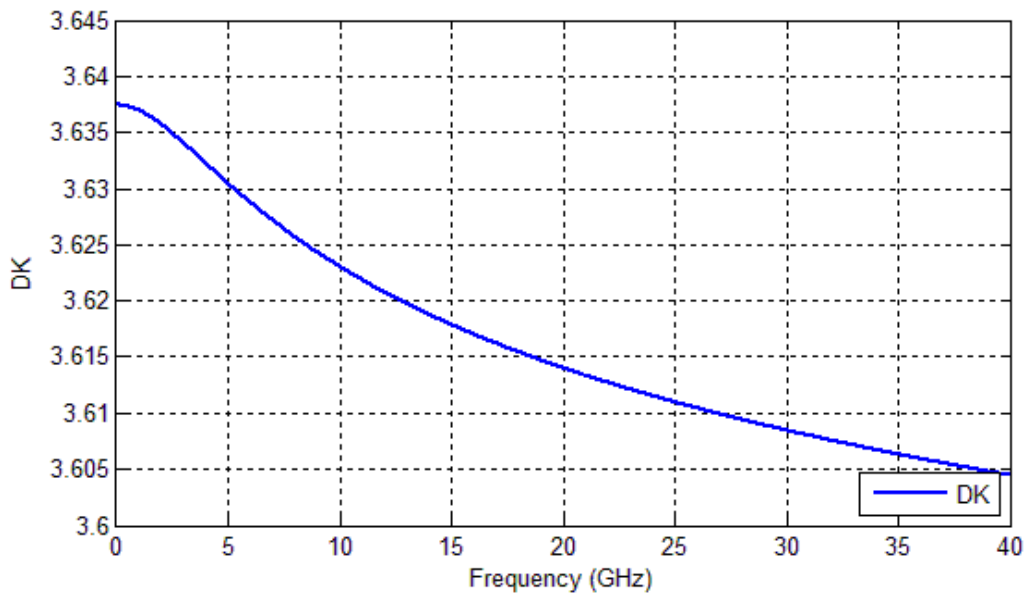


Figure 31. Extracted DK2 (light blue layer).

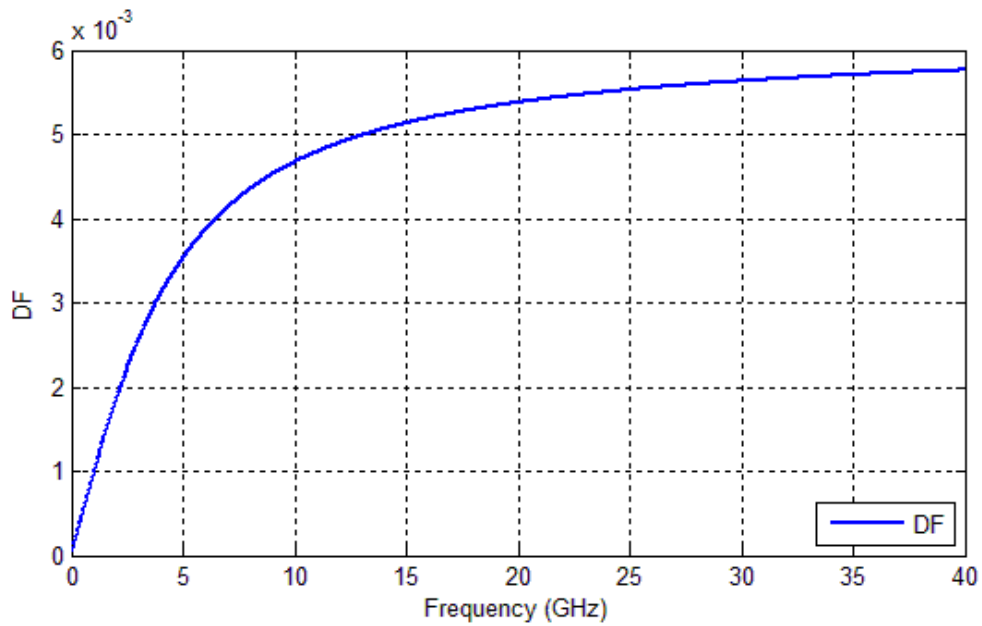


Figure 32. Extracted DF2 (light blue layer).

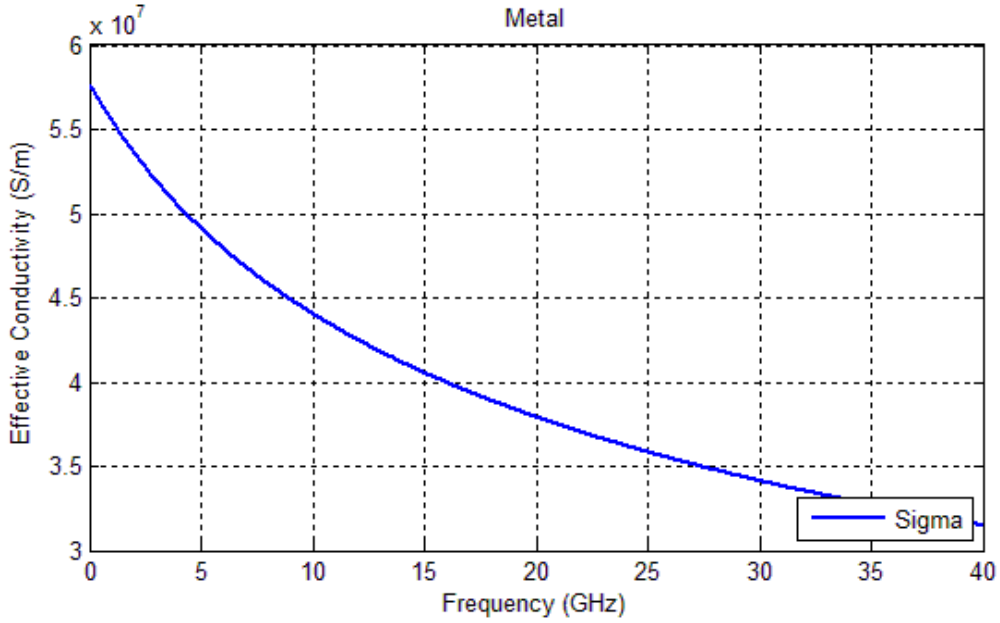


Figure 33. Extracted effective conductivity of signal and ground.

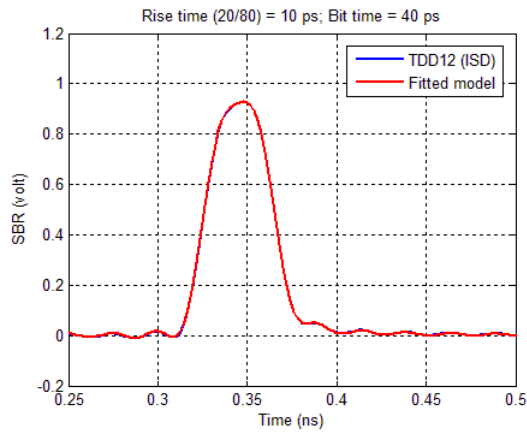


Figure 34. Measured vs. fitted single-bit response.

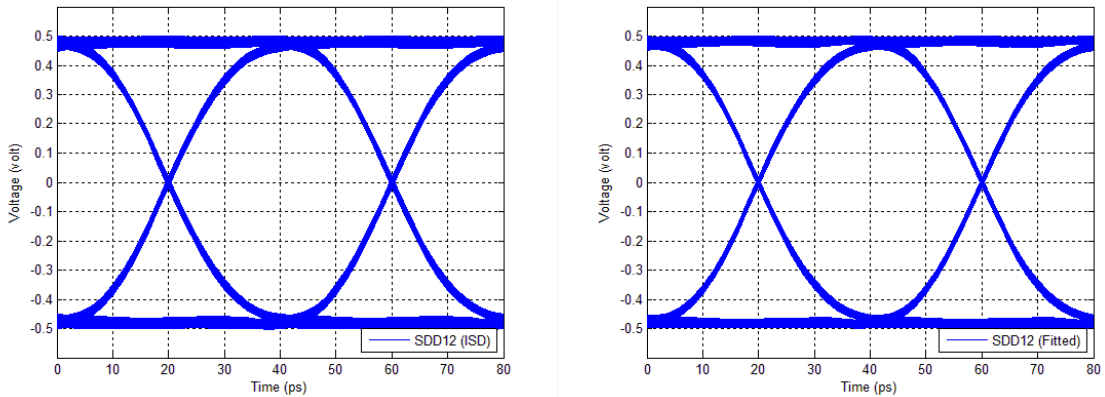


Figure 35. Measured vs. fitted eye diagram at 25 Gbps and 10 ps rise time (20/80) for PRBS12.

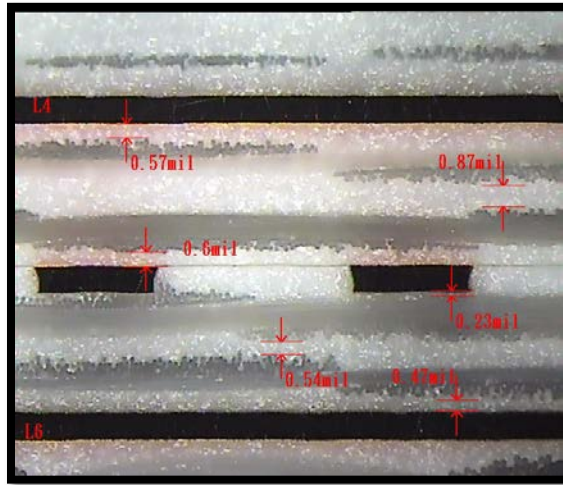


Figure 36. PCB cross section of the stripline characterized.

6. Conclusion

The main challenge in characterizing PCB interconnects is the sheer volume of data to be analyzed considering a plethora of dielectric material choices, trace design options, PCB layer count and fabrication processes. To address this challenge, we proposed a methodology and algorithms to analyze PCB interconnects, document the results and generate necessary models in automated fashion. The documented results include such key interconnect parameters as insertion loss per inch, trace impedance, DK and DF of dielectric and copper surface roughness. A methodology, which is based on minimal reflected energy, was developed to define a single number for non-uniform trace impedance. This paper shows that DK, DF and surface roughness models can be extracted to simultaneously fit all single-ended, differential-mode and common-mode IL, RL, NEXT, FEXT and TDR/TDT. This paper also shows that both magnitude and phase of FEXT have significant impact on the extracted DK values and ignoring it will lead to incorrect results.

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